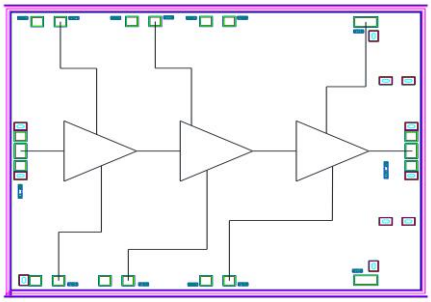
TFPA369-H
2 GHz ~ 6 GHz GaAs MMIC Power Amplifier Chip

★1.Product Features

- Frequency Range: 2 GHz ~ 6 GHz
- Gain: 32 dB
- OP1dB: 34 dBm
- PAE@OP1dB: 40%
- Input Return Loss: -10 dB
- Output Return Loss: -10 dB
- Die Size: 3.60 × 3.00 × 0.100 mm^3

Functional Block Diagram



★2.Product Introduction

The TFPA369-H is a wideband GaAs power amplifier die covering an operating frequency of 2 GHz ~ 6 GHz. The chip adopts dual-power-supply operation, with typical operating voltages of VD=+8 V and VG=-0.8 V. In continuous wave (CW) mode it provides 32 dB small-signal gain and 34 dBm output power at 1 dB gain compression, together with 40% typical power added efficiency. The chip can be applied in radar microwave transceiver modules and high-power solid-state transmitters, and is fabricated with domestic processes to meet localization requirements.

The backside of the die is metallized, suitable for eutectic sintering. The chip adopts an on-chip metallized via-hole process to ensure good grounding, which makes it simple and convenient to use without additional grounding measures.

★3.Typical Electrical Characteristics

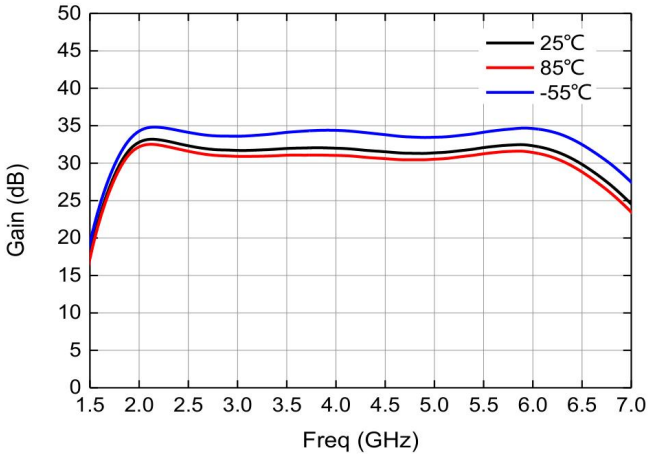
TA=+25℃, CW, 50Ω system

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Frequency	Freq	2	-	6	GHz
Gain	Gain	30	32	-	dB
Gain Flatness	δGain	-	±1.0	-	dB
Output 1dB Compression Point Power	OP1dB	-	34.0	-	dBm
Power Added Efficiency @ OP1dB	PAE	30	40	-	%
Input Return Loss	RL_in	-10	-12	-	dB
Output Return Loss	RL_out	-10	-12	-	dB
Operating Voltage	VD	+6	+8	-	V
Quiescent Current*	IDQ	-	800	-	mA

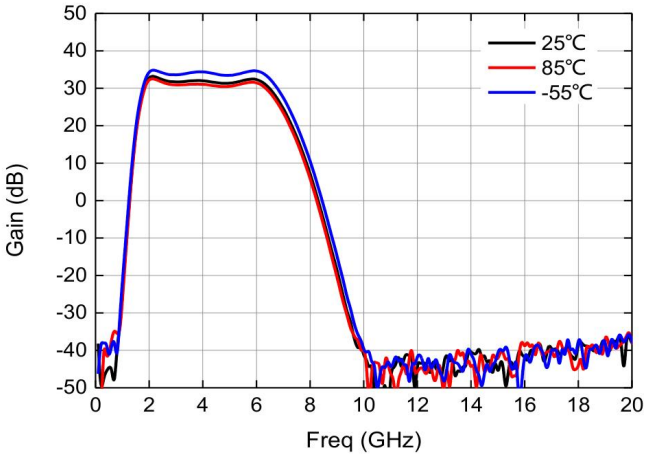
* VG=-0.8 V by default.
In actual use, the VG voltage shall be fine-tuned so that the quiescent current IDQ=800 mA.

Email: ttf@ttfelectronic.com
Website:ttfelectronic.com
Address: Building 16, Area C, Entrepreneurship and R&D Park, Xi'an High-tech Industrial Development Zone, China

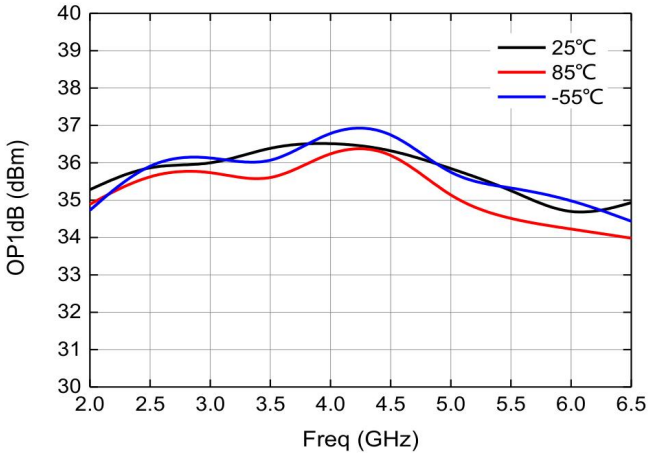
★4.Typical Test Curves



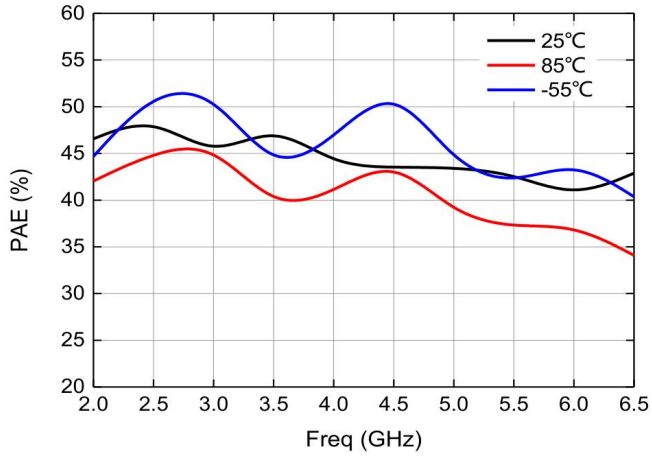
Small-Signal Gain vs. Frequency



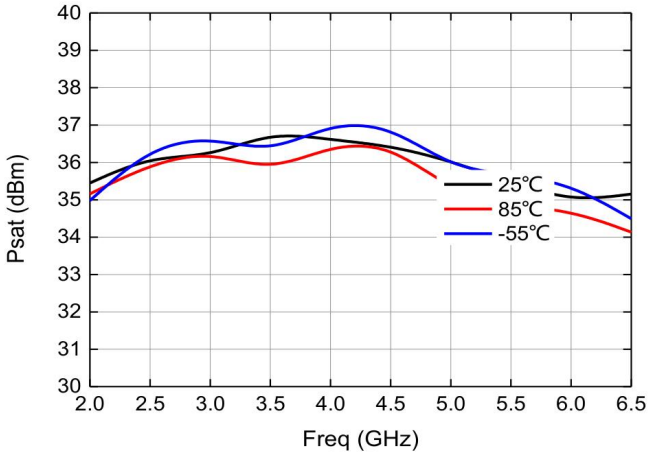
Small-Signal Gain vs. Frequency



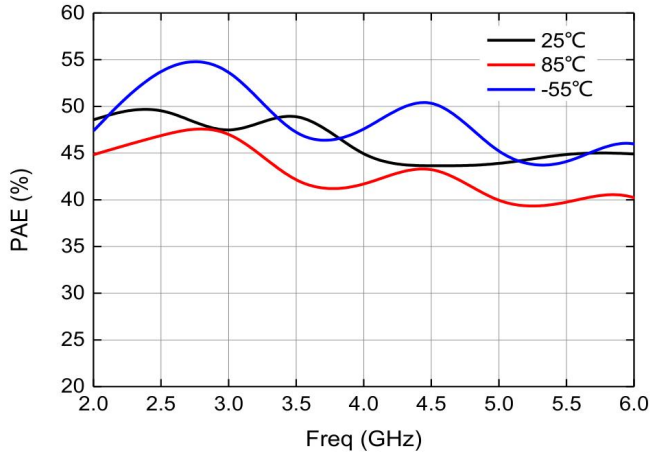
OP1dB vs. Frequency



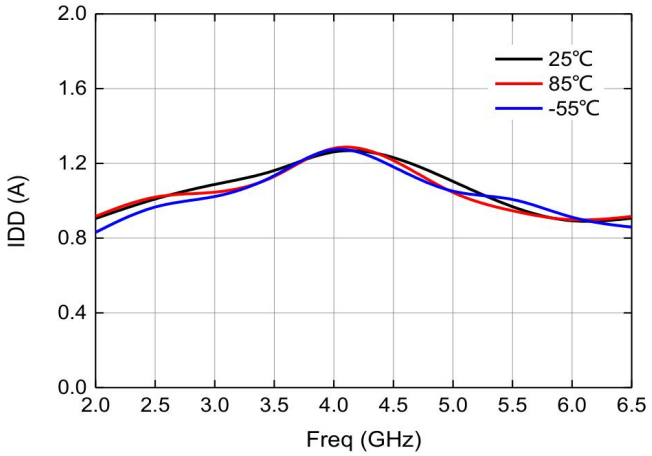
PAE@OP1dB vs. Frequency



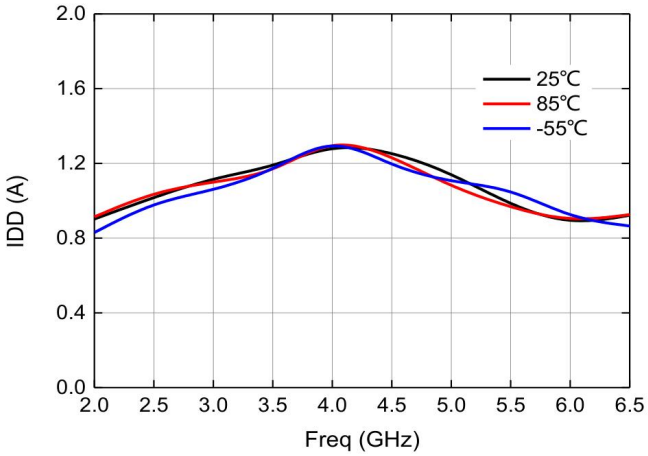
Psat vs. Frequency



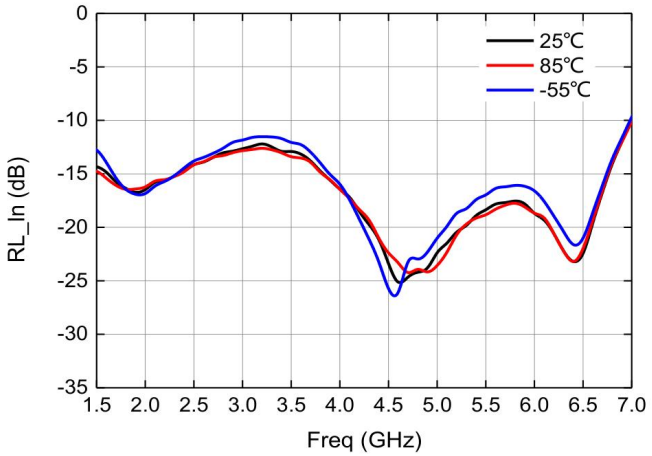
PAE@Psat vs. Frequency



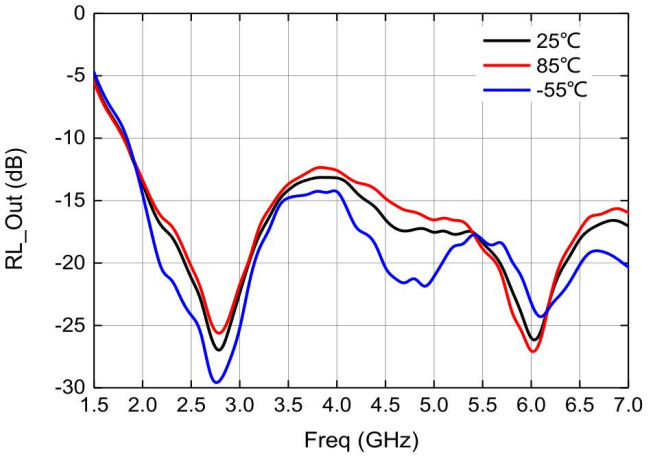
IDD@OP1dB vs. Frequency



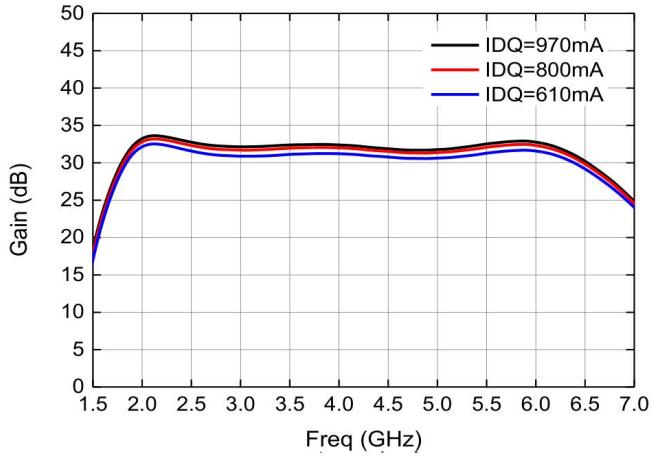
IDD@Psat vs. Frequency



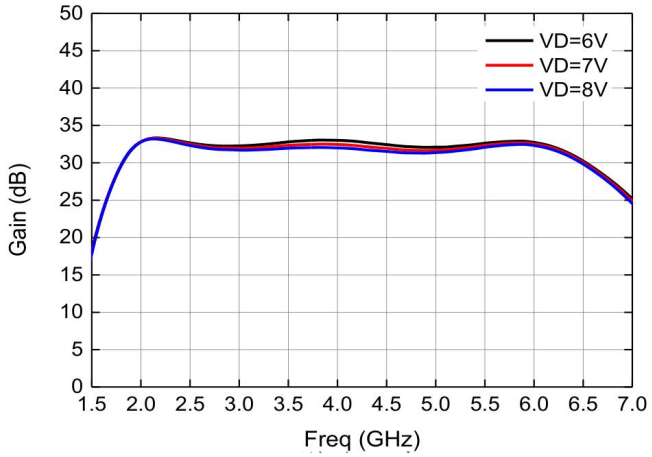
Input Return Loss vs. Frequency



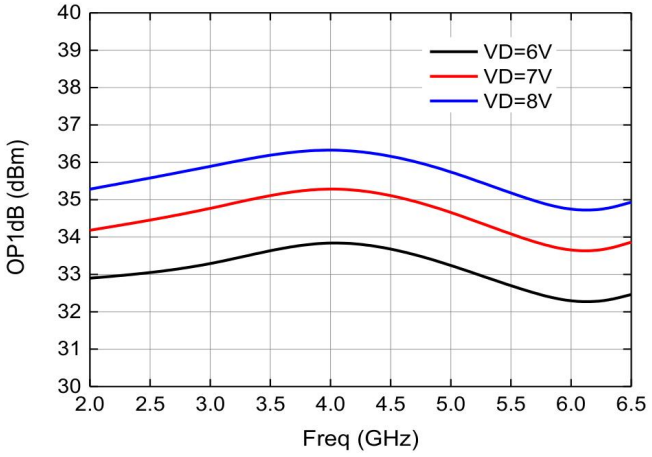
Output Return Loss vs. Frequency



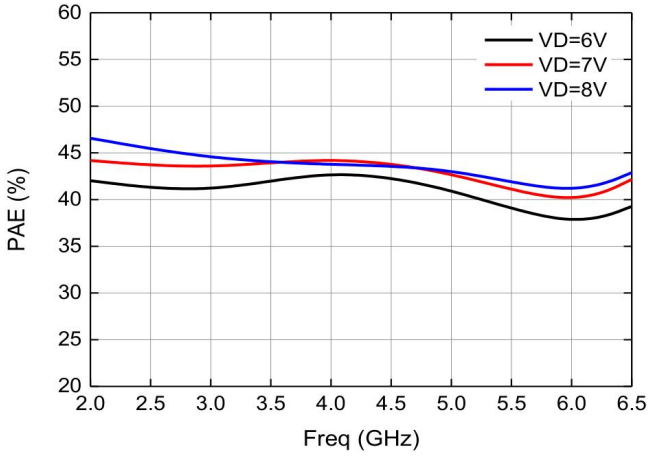
Small-Signal Gain vs. Frequency @VD=8V



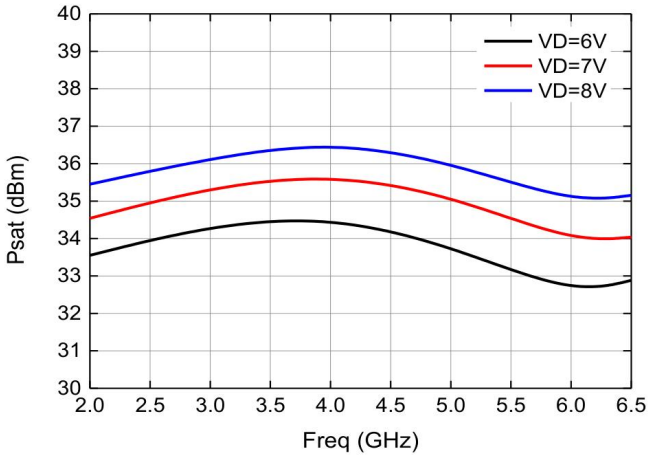
Small-Signal Gain vs. Frequency @VG=-0.8V



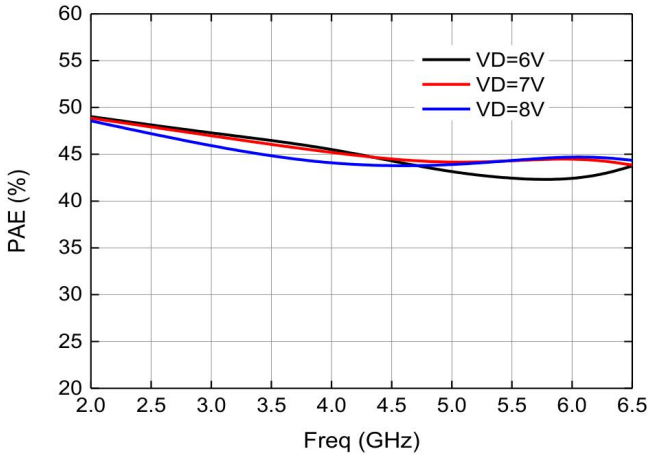
OP1dB vs. Frequency @VG=-0.8V



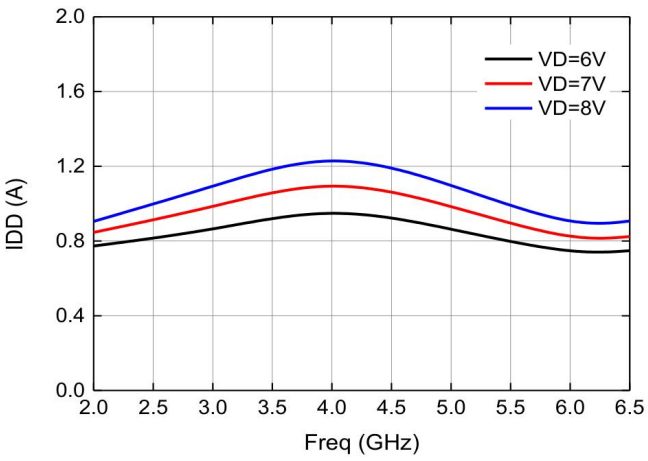
PAE@OP1dB vs. Frequency @VG=-0.8V



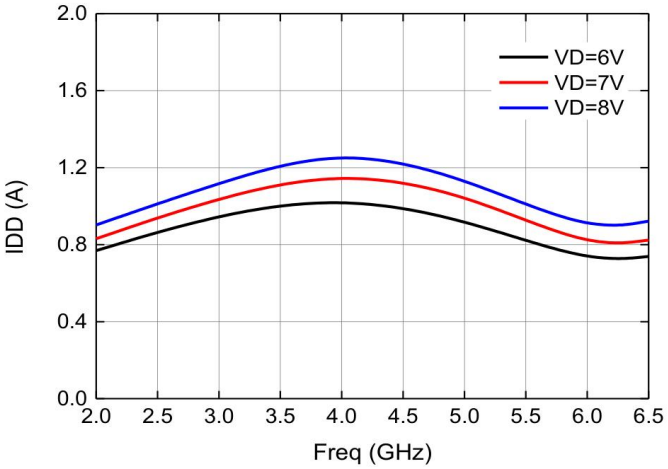
Psat vs. Frequency @VG=-0.8V



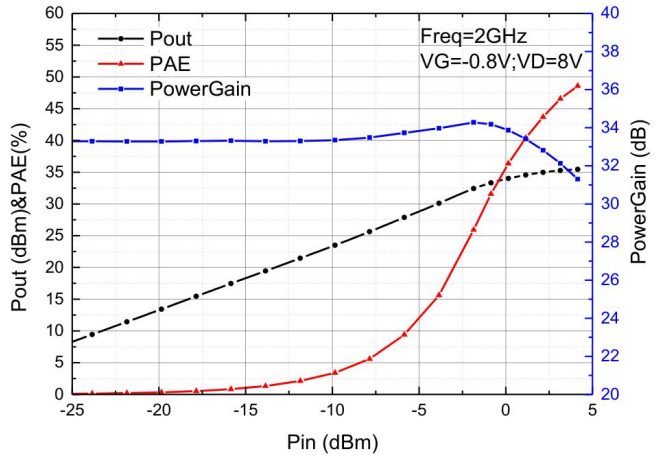
PAE@Psat vs. Frequency @VG=-0.8V



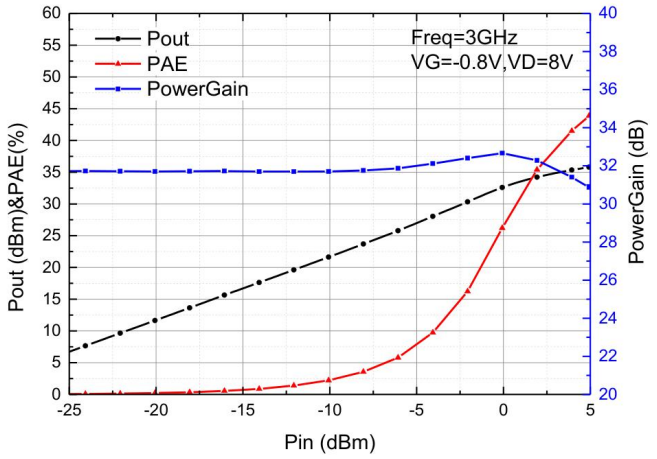
IDD@OP1dB vs. Frequency @VG=-0.8V



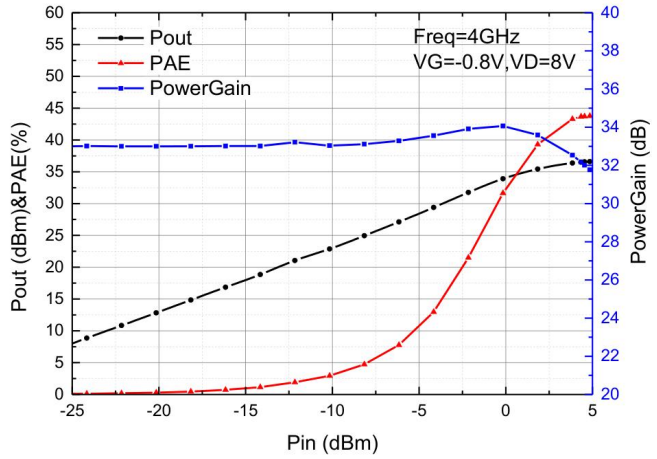
IDD@Psat vs. Frequency @VG=-0.8V



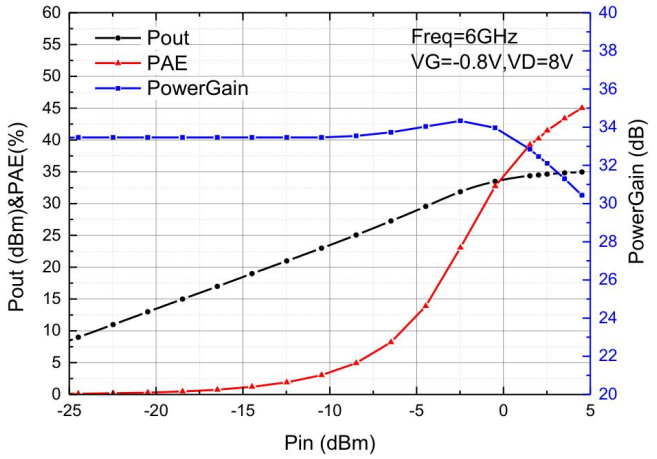
Power Sweep @Freq=2 GHz



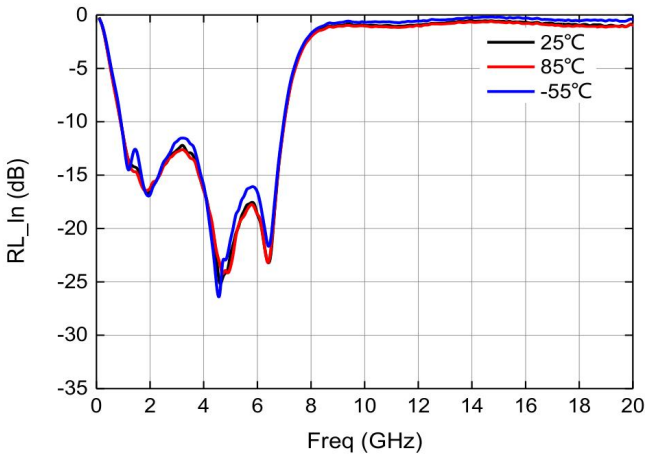
Power Sweep @Freq=3 GHz



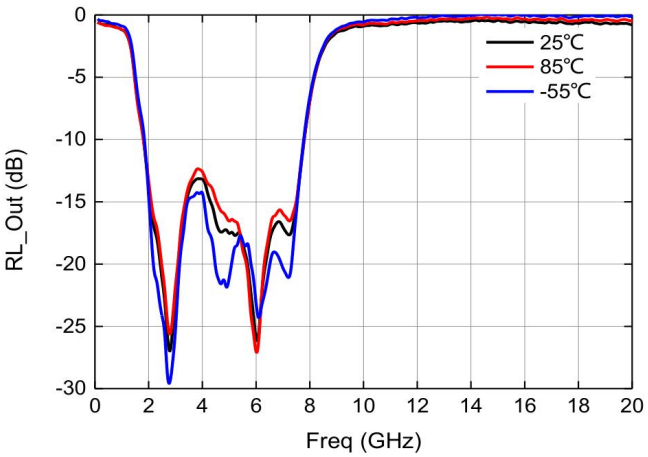
Power Sweep @Freq=4 GHz



Power Sweep @Freq=6 GHz



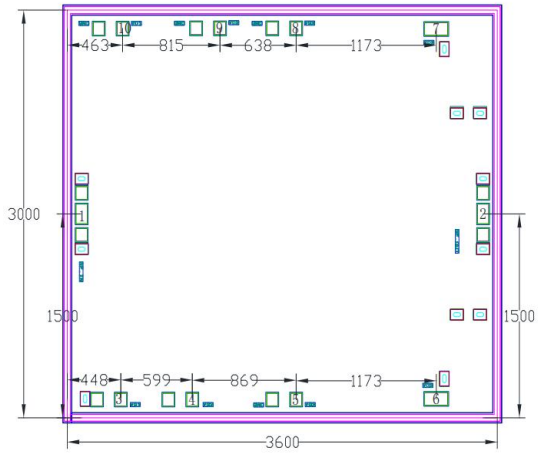
Input Return Loss vs. Frequency
(Pin=-20 dBm, VG=-0.8V, VD=8V)



Output Return Loss vs. Frequency
(Pin=-20 dBm, VG=-0.8V, VD=8V)

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★5.Outline Dimensions



Notes:

1. Unit: μm
2. The backside of the die is gold-plated and grounded.
3. RF pad size: 150 μm × 100 μm
4. VD3 pad size: 200 μm × 100 μm
5. Other pad size: 100 μm × 100 μm
6. Outline dimension tolerance: ±50 μm

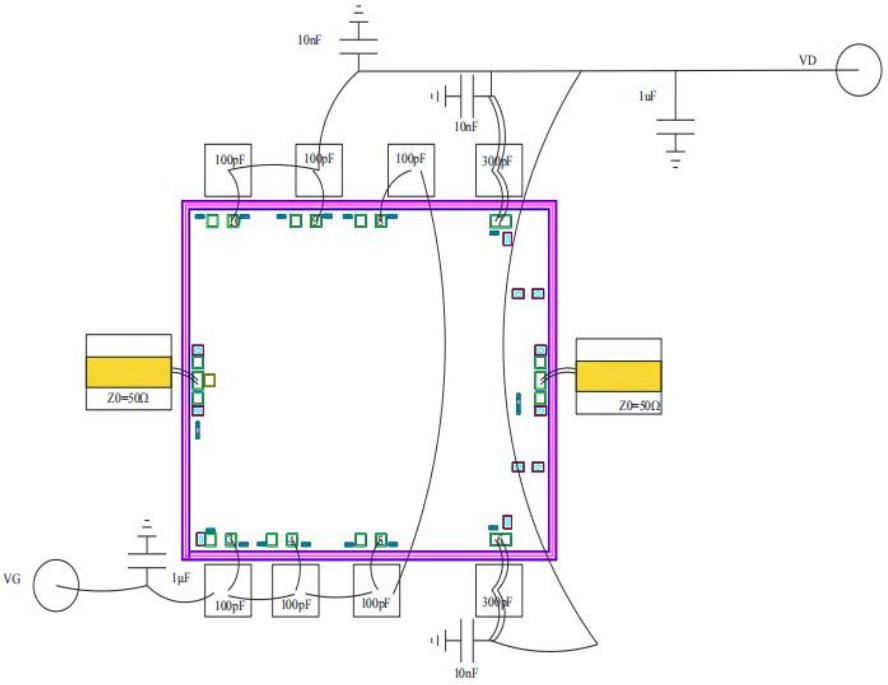
★6.Bond Pad Definition

Pressure Point Number	Function Definition	Function Description
1	RFin	RF signal input; connect to 50 Ω system, with on-chip DC blocking
2	RFout	RF signal output; connect to 50 Ω system, with on-chip DC blocking
3	VG1	Gate voltage supply terminal 1
4	VG2	Gate voltage supply terminal 2
5, 8	VG3	Gate voltage supply terminal 3
6, 7	VD3	Drain voltage feed terminal 3
9	VD2	Drain voltage supply terminal 2
10	VD1	Drain voltage supply terminal 1

★7.Reference Circuit

Instructions for Use:

1. Molybdenum-copper is recommended as the carrier; gold-tin sintering is preferred to ensure good heat dissipation and grounding.
2. The RF input port is bonded with 2 gold wires of 25 μm diameter, and the RF output port with 2 wires of 25 μm diameter; the span shall not exceed 300 μm.
3. The 100 pF capacitors are on-chip capacitors, the 10 nF capacitors are ceramic filter capacitors, and the 1 μF capacitor is the power supply filter capacitor, whose withstand voltage shall be greater than 20 V.
4. Pay attention to thermal design to prevent the chip junction temperature from being too high.



Note: Although this chip has high stability, due to its high gain there may be environmental feedback loops in system use; when the ripple of the power supply system is large, the number of power supply filtering stages and the power supply filter capacitance shall be increased.

★8. Precautions

Absolute Maximum Ratings	Numerical value
Input Power Pin, 50 Ω	10 dBm
Drain Voltage	+10 V
Storage Temperature	-65℃ ~ +150℃
Operating Temperature	-55 ~ +85℃
Sintering Temperature (30 s, N2)	300℃
Exceeding the above conditions may cause permanent damage to the chip.	



This product is sensitive to static electricity.
Please take precautions against static electricity during use.