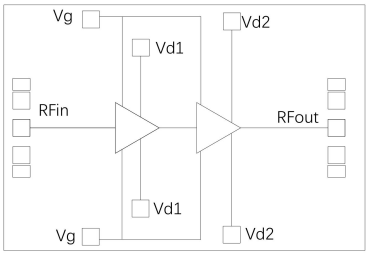
★1.Product Features

- Frequency range: 4.0 ~ 8.0 GHz
- Psat: 43 dBm
- Power gain: 13 dB
- Power supply: 28 V / 420 mA
- 50 ohm input / output
- Chip dimensions: 3.3 mm × 2.5 mm × 0.1 mm

Functional Block Diagram



★2.Product Introduction

TFPA3004 is a power amplifier chip fabricated with the GaN pHEMT process. It covers the 4.0 ~ 8.0 GHz frequency range and delivers 13 dB power gain with a saturated output power of 43 dBm at a 28 V supply. The chip is grounded through backside vias. It is mainly used in communication systems, high-power transmit/receive modules and other fields.

★3.DC Electrical Parameters (TA=+25℃)

Item	Min.	Typ.	Max.	Unit
Gate bias voltage	—	-2.2	—	V
Drain operating voltage	—	28	—	V
Quiescent drain current	—	420	—	mA
Dynamic drain current	—	2000	—	mA

★4.Microwave Electrical Parameters (TA=+25℃, Vd=+28V, 300 μs, 30%)

Item	Min.	Typ.	Max.	Unit
Frequency range	4.0 ~ 8.0			GHz
Saturated output power Psat	—	43	—	dBm
Power added efficiency PAE	—	40	—	%
Power gain	—	13	—	dB
Power gain flatness	—	±0.5	—	dB
Input / output return loss	—	-14	—	dB

Email: ttf@ttfelectronic.com
Website:ttfelectronic.com
Address: Building 16, Area C, Entrepreneurship and R&D Park, Xi'an High-tech Industrial Development Zone, China

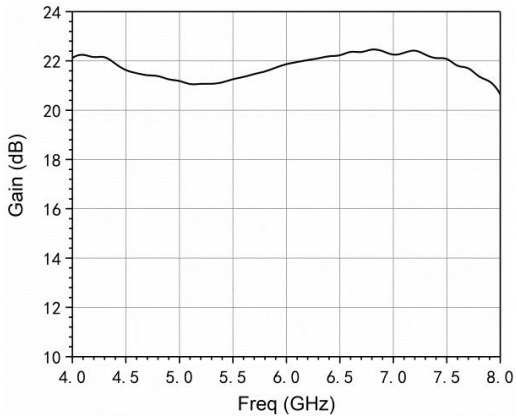
★5.Absolute Maximum Ratings

Parameter	Limit value
Maximum drain voltage	+30 V
Maximum input power	+30 dBm
Operating temperature	-55 ℃ ~ +85 ℃
Storage temperature	-65 ℃ ~ +120 ℃

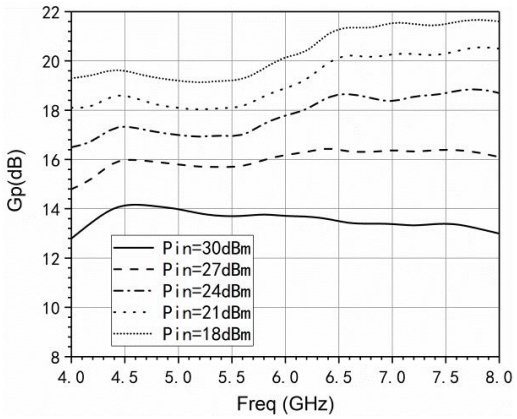
[1] Exceeding any one of the above maximum limits may cause permanent damage.

★6.Typical Test Curves (Vd=+28V, 300 μs, 30%)

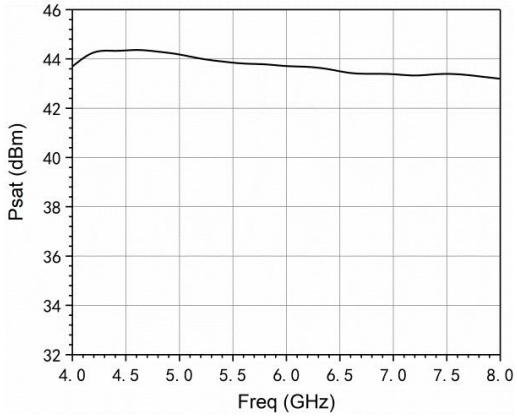
Gain vs. frequency (@Pin=-25 dBm)



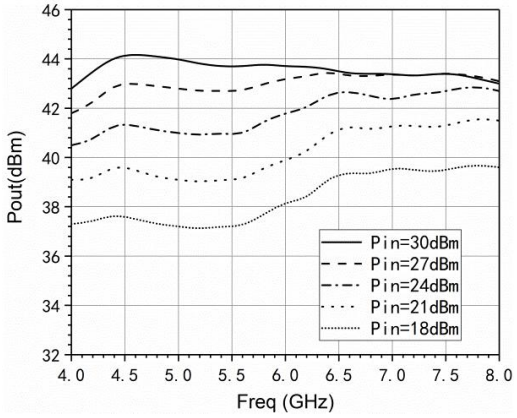
Power gain vs. frequency



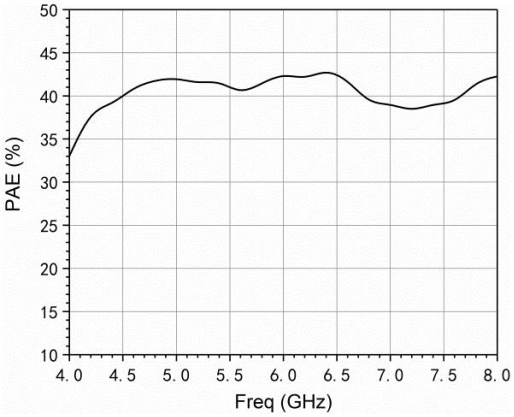
Saturated output power vs. frequency



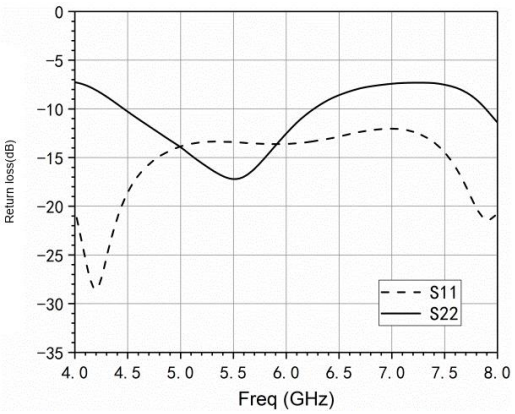
Output power vs. frequency



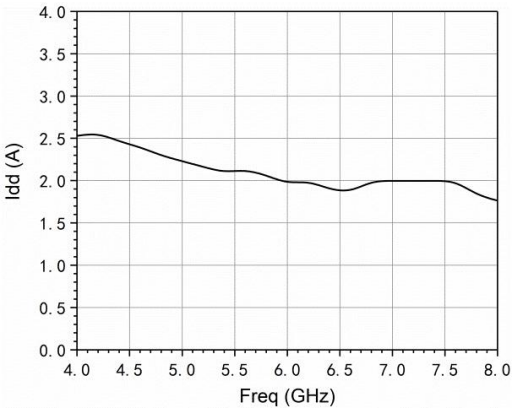
Power added efficiency vs. frequency (@Psat)



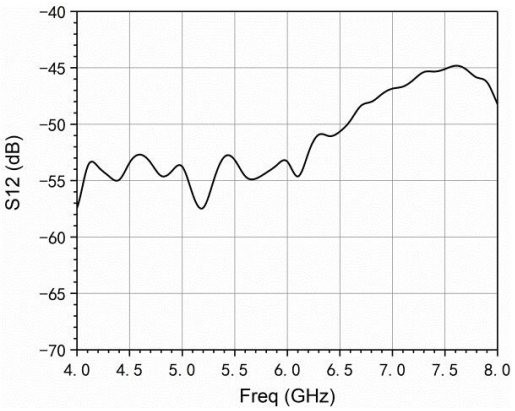
Return loss vs. frequency



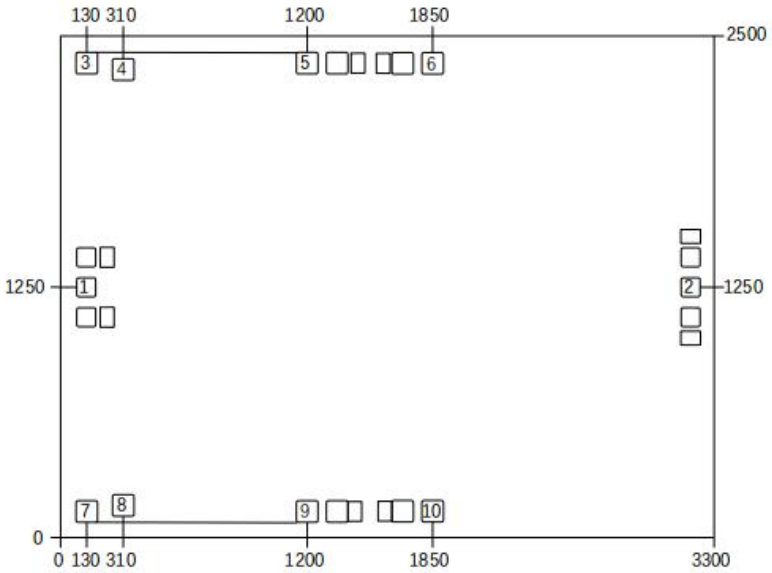
Idd vs. frequency



Reverse isolation vs. frequency (@Psat)



★7.Outline Dimensions

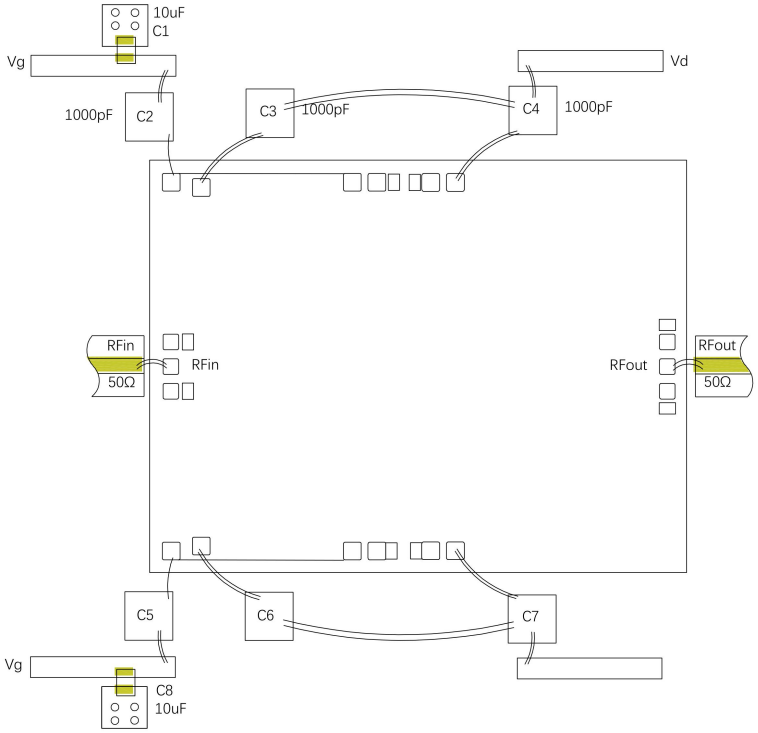


Notes:
1. Unit: μm
2. Bonding pads are gold-plated
3. Dimension tolerance: ± 20 μm

★8.Bonding Pad Definition

Pad No.	Function	Description	Size
1	IN	RF signal input, connected to an external 50 Ω system, no external DC blocking capacitor required	100 × 100 μm
2	OUT	RF signal output, connected to an external 50 Ω system, no external DC blocking capacitor required	100 × 100 μm
4,6,8,10	Vd	Drain supply port of the chip, supply voltage 28 V	100 × 100 μm
3,5,7,9	Vg	Gate supply port of the chip, voltage -2.2 V, quiescent current 400 mA	100 × 100 μm

★9.Suggested Assembly Diagram



Note: C2, C3, C4, C5, C6 and C7 are 1000 pF single-layer ceramic capacitors. To ensure more stable performance of the amplifier, it is recommended to solder ceramic capacitors with the capacitance values shown in the assembly diagram at the power supply terminals for filtering. The number of filter capacitors or combinations of different capacitance values may also be increased according to actual requirements.

★10.Precautions

1. Assemble and use in a clean environment. Store in an ESD-protective container and keep dry.
2. The backside of the chip is gold-plated for grounding. Ensure that the backside is in full contact with ground and properly grounded during use.
3. Sinter with AuSn solder at a ratio of 80/20. The sintering temperature shall not exceed 300 ℃ and the sintering time shall be as short as possible, not exceeding 20 s.
4. This product is an ESD-sensitive device. Observe ESD precautions during storage and use.
5. Do not attempt to clean the chip surface with dry or wet chemical methods.
6. Please contact the supplier if you have any questions.



This product is sensitive to static electricity.
Please take precautions against static electricity during use.