★1. Product Overview

The TFMUL2433P is an x2 active broadband frequency multiplier using GaAs PHEMT technology in a 3.0 mm × 3.0 mm leadless surface-mount ceramic package. Driven by a +3 dBm signal it delivers +17 dBm of typical output power (bare die) over an output frequency range of 24 GHz to 33 GHz. At 28 GHz the Fo and 3Fo isolation are greater than 25 dBc and 36 dBc respectively. The TFMUL2433P targets the local-oscillator multiplier chain of point-to-point microwave radios and VSAT RF systems, and reduces component count significantly compared with conventional multiplier schemes. Its low added SSB phase noise of −132 dBc/Hz at 100 kHz offset helps preserve good system noise performance. Input/output 50 Ω matching and DC blocking are already implemented inside the package, which removes the secondary assembly and wire-bonding steps so that the device can be assembled directly with surface-mount processes.

Input/output 50 Ω matching and DC blocking are implemented internally, so the device can be connected directly to a 50 Ω system.

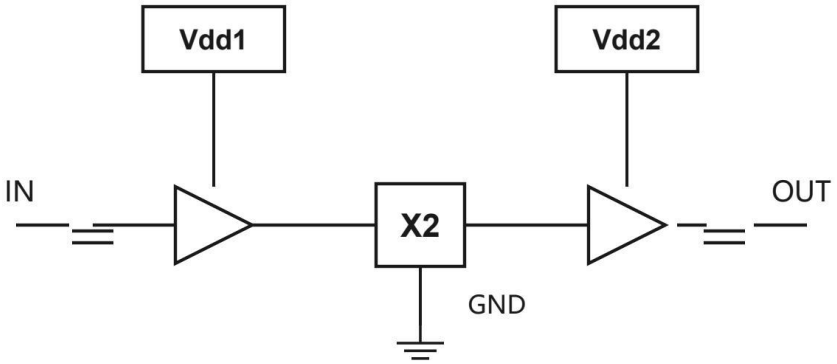


Figure 1. Functional Block Diagram

★2. Key Features

- High output power: +17 dBm (3 dBm drive, bare-die typical)
- Single supply: +5 V @ 85 mA
- Low input drive level: 0 to +6 dBm
- 3 × 3 mm, 12-lead surface-mount ceramic package, RoHS compliant
- Fo isolation: > 25 dBc; 3Fo isolation: > 36 dBc @ Fout = 28 GHz
- Input/output internally 50 Ω matched and DC-blocked; no wire bonding required
- 100 kHz SSB phase noise: −132 dBc/Hz

★3. Typical Electrical Parameters

TA = +25 °C, Vdd1 and Vdd2 = +5 V, input drive 3 dBm.

Table 1. Typical Electrical Parameters

Parameter	Min.	Typ.	Max.	Unit
Input frequency range	12	—	16.5	GHz
Output frequency range	24	—	33	GHz
Output power	12	17	—	dBm
Fo isolation (relative to output level)	—	22	—	dBc
3Fo isolation (relative to output level)	—	35	—	dBc
Input return loss	10	—	—	dB
Output return loss	15	—	—	dB
SSB phase noise (100 kHz offset)	—	−132	—	dBc/Hz
Supply current (Idd1 + Idd2)	—	85	—	mA

Note :

The table lists bare-die measured typical data. The estimated additional loss of the package interconnect (wire bonds and cavity transmission lines) is ≤0.5 dB; the final guaranteed specification of the packaged sample is subject to the packaged-sample test report.

Before the packaged-sample verification data in this document is updated, the electrical parameter table is bare-die measured data (see Note 1).

★4. Typical Operating Characteristics

Bare-die measured data at TA = +25 °C unless otherwise noted; the packaged typical curves will be updated during sample verification.

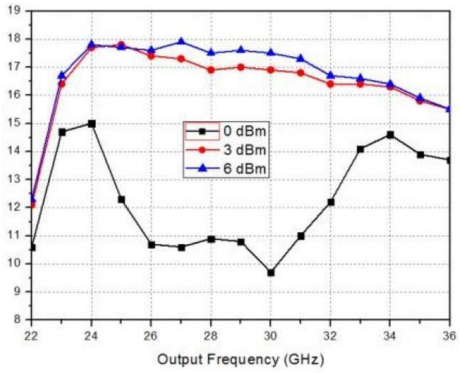


Figure 2. Output Power vs. Drive Level

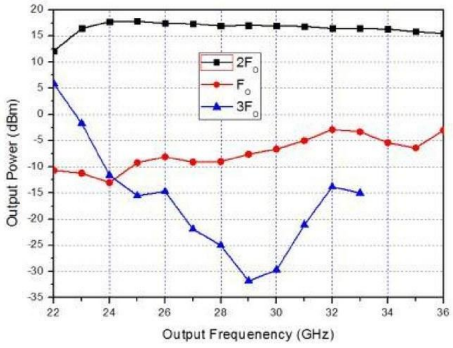


Figure 3. Isolation @ 3 dBm Drive Level

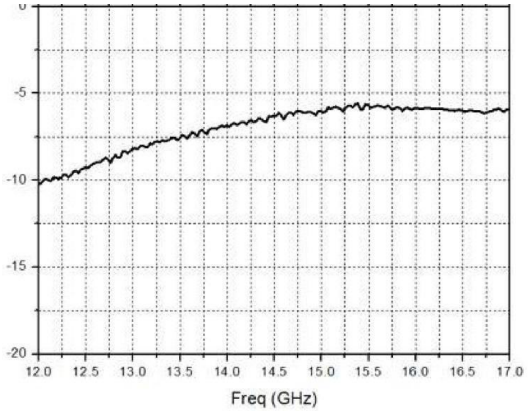


Figure 4. Input Return Loss vs. Temperature

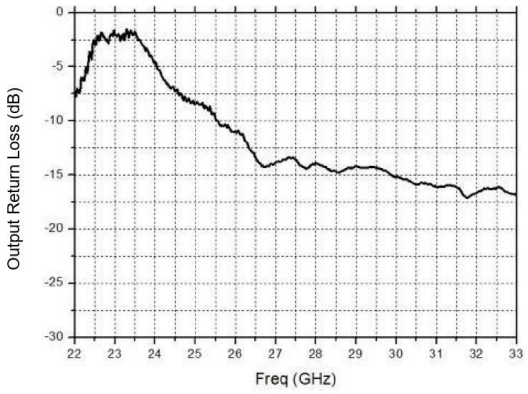


Figure 5. Output Return Loss vs. Temperature

★5. Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Value
RF input power (Vdd = +5 V)	+13 dBm
Supply voltage (Vdd1, Vdd2)	+6.0 Vdc
Channel temperature	175 °C
Continuous dissipation (T = 85 °C, bare die)	703 mW (derate 7.8 mW/°C above 85 °C)
Thermal resistance (channel to package ground pad)	≈135 °C/W (estimated[1])
Storage temperature	−65 to +150 °C
Operating temperature	−55 to +85 °C

Estimated from a bare-die thermal resistance of 128 °C/W (channel to die backside) plus the package interface resistance; subject to sample measurement.

This is an electrostatic-sensitive device (ESD); observe ESD precautions when handling. Exceeding the ratings above may cause permanent damage.

★6. Package Outline

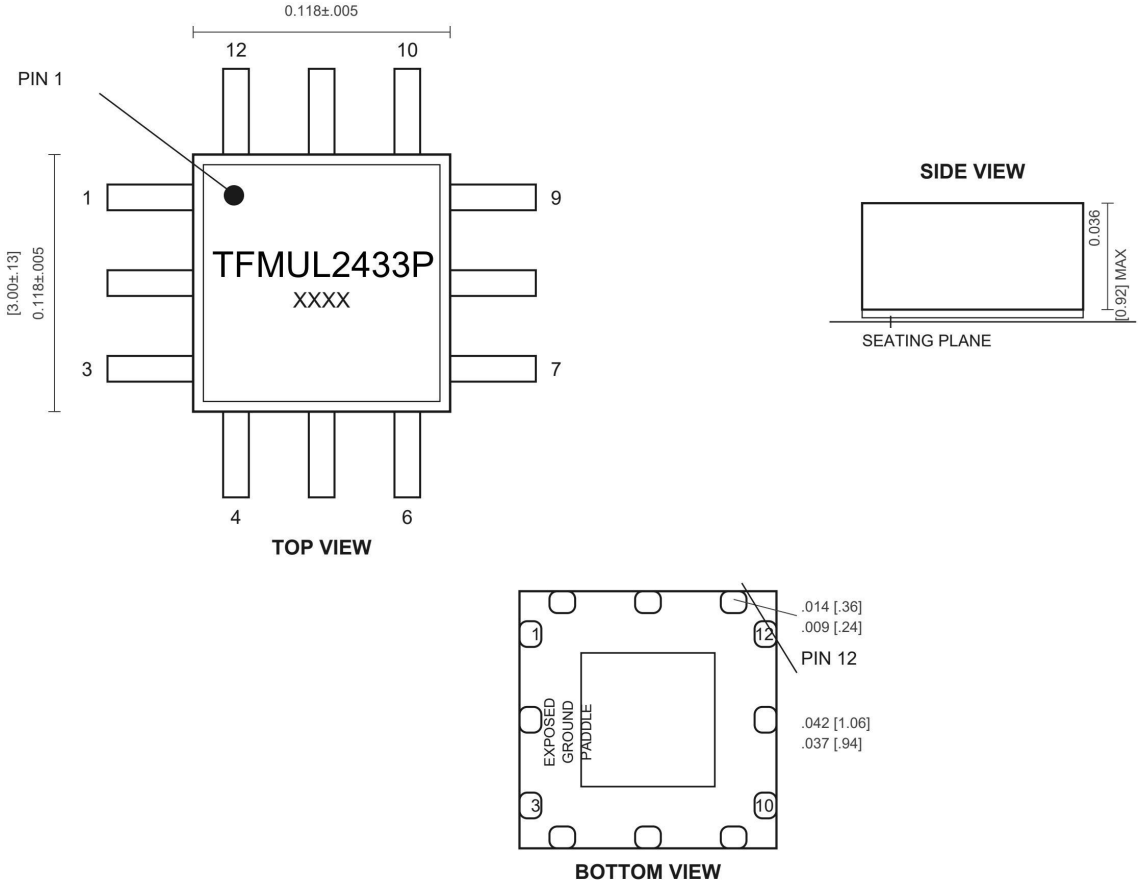


Figure 6. Package Outline Drawing (unit: inch [mm])

Note: the package body is alumina ceramic; the leads and the bottom ground pad are gold over nickel; lead-spacing tolerances are non-cumulative; package warpage ≤0.05 mm; all ground leads and the bottom ground pad must be soldered to the PCB RF ground. Refer to the formal package drawing for detailed mechanical dimensions.

★7. Pin Description

Table 3. Pin Description

Pin No.	Symbol	Description
1, 3, 7, 9	GND	Ground; the bottom ground pad of the package must also be connected to RF/DC ground
2	RFIN	Internally DC-blocked; matched to 50 Ω over 12–16.5 GHz
4, 5, 6, 11	N/C	Not internally connected; grounding them in the application is recommended for better isolation and heat dissipation
8	RFOUT	Internally DC-blocked; matched to 50 Ω over 24–33 GHz
10	Vdd2	Supply voltage +5 V ± 0.5 V
12	Vdd1	Supply voltage +5 V ± 0.5 V

★8. Application Circuit

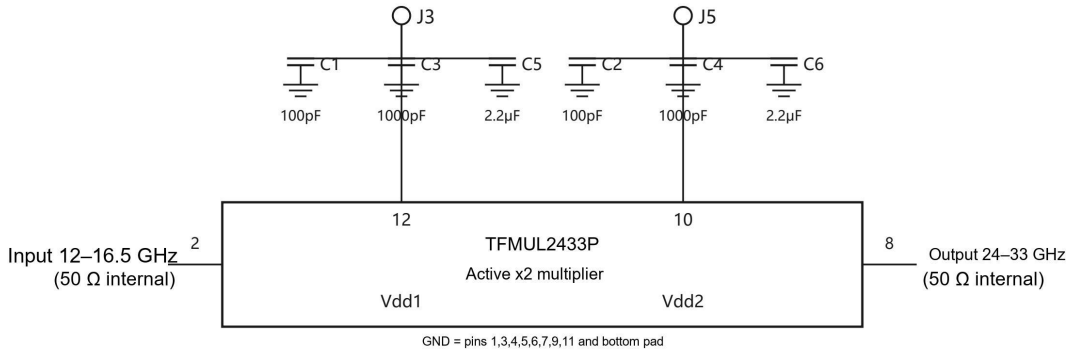


Figure 7. Application Circuit

Each supply pin requires external 100 pF, 1,000 pF and 2.2 μF bypass capacitors to ground; keep the PCB RF traces at 50 Ω impedance, and connect the ground leads and the bottom pad directly to the ground plane through via arrays.

Table 4. External Components

Component	Value
C1, C2	100 pF
C3, C4	1,000 pF
C5, C6	2.2 μF

★9. Package Information

Table 5. Package Information

Model	Package body	Lead plating	MSL	Package marking
TFMUL2433P	Alumina ceramic (white)	Gold over nickel	MSL3	TFMUL2433P / lot code

Reflow soldering peak temperature 260 °C.

★10. Ordering Information

Table 6. Ordering Information

Ordering model	Form	Package	Description
TFMUL2433P	Packaged product	3 × 3 mm 12-lead SMT ceramic package	Pin-to-pin surface-mount product, output 24–33 GHz
TFMUL2433P-EVB	Evaluation board	Rogers 4350 evaluation board	Includes all decoupling capacitors and K connectors (optional)

★11. Revision History

Table 7. Revision History

Version	Date	Description
Rev0.1	2026-10	Initial release; packaged-sample verification data pending update

★12. Important Notice

The final guaranteed specifications of the packaged product described in this document are subject to the formal sample test report. Operating the device beyond the rated conditions given in this data sheet may damage it.