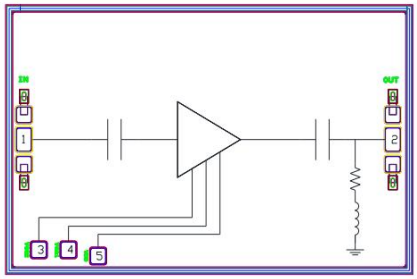
★1.Product Features

- Frequency range: 1~11 GHz
- Noise figure: 1.8 dB
- Gain: 15 dB
- Output P-1dB: 18.5 dBm
- Operating current: 45 mA @ +5 V/+1.5 V/-0.47 V
- Chip size: 2.7 mm × 1.7 mm × 0.1 mm
- Replacement for: HMC753

Functional Block Diagram



★2.Product Introduction

The TFLN1018-H is a low noise amplifier chip operating in the 1~11 GHz frequency range with a drain voltage of +5 V. At a current of 45 mA, it provides a gain of 14 dB, an output P-1dB of 18.5 dBm and a typical noise figure of 1.8 dB. The chip is fabricated domestically and can meet the requirements of localized applications. It is available as a replacement for the foreign model HMC753.

The chip backside is metallized and is suitable for conductive adhesive die attachment or eutectic bonding. The chip adopts an on-chip metallized via-hole process to ensure good grounding, which makes it easy to use without additional grounding measures.

★3.Electrical Characteristics

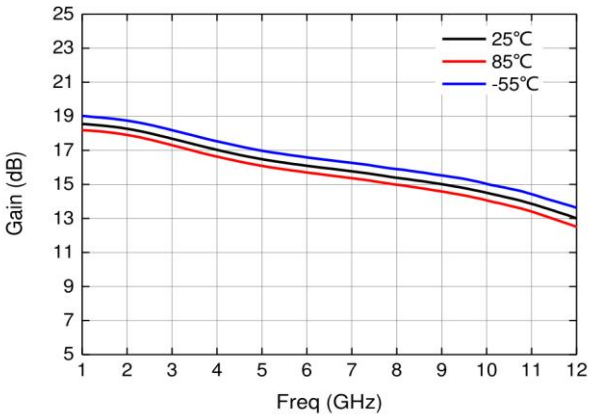
TA=+25℃, 50Ω System,VDD=+5V, VGG1=-0.47V, VGG2=+1.5V

Parameter	Symbol	Min	Typ	Max	Unit
Operating Frequency	Freq	1	—	11	GHz
Gain	Gain	—	15	—	dB
Output P-1dB	OP1dB	—	18.5	—	dBm
Saturated Output Power	Psat	—	20	—	dBm
Input Return Loss	RL_in	—	-10	—	dB
Output Return Loss	RL_out	—	-14	—	dB
Noise Figure	NF	—	1.8	—	dB
Output Third-Order Intercept	OIP3	—	30	—	dBm
Quiescent Current	IDQ	—	45	—	mA

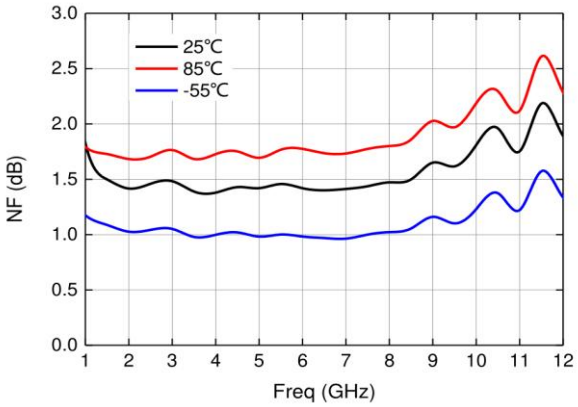
Email: ttf@ttfelectronic.com
Website:ttfelectronic.com
Address: Building 16, Area C, Entrepreneurship and R&D Park, Xi'an High-tech Industrial Development Zone, China

★4.Typical Test Curve

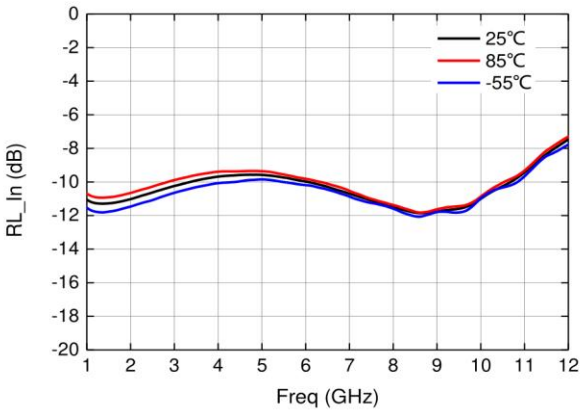
Gain vs. Frequency



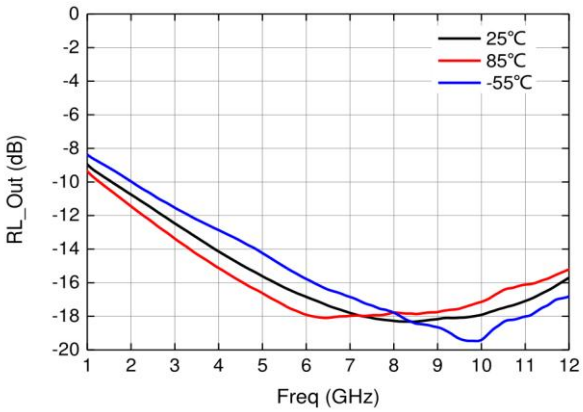
Noise Figure vs. Frequency



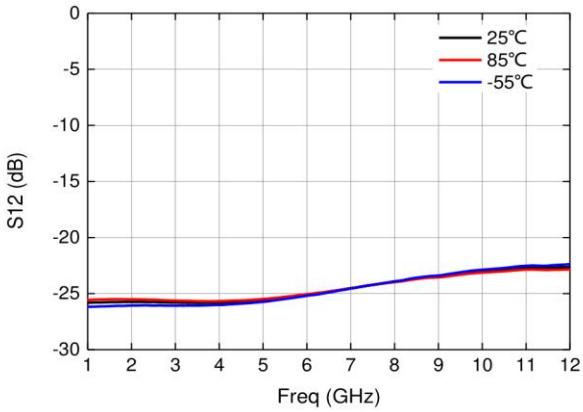
Input Return Loss vs. Frequency



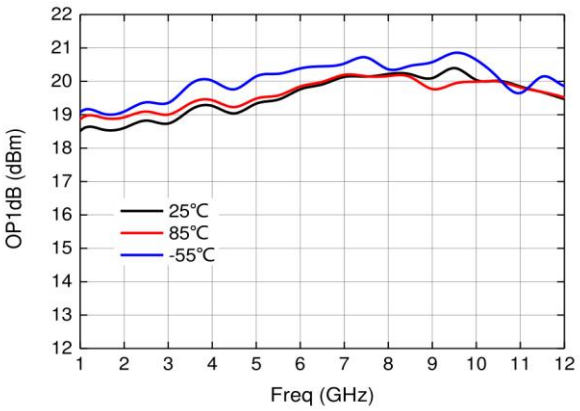
Output Return Loss vs. Frequency



Reverse Isolation vs. Frequency

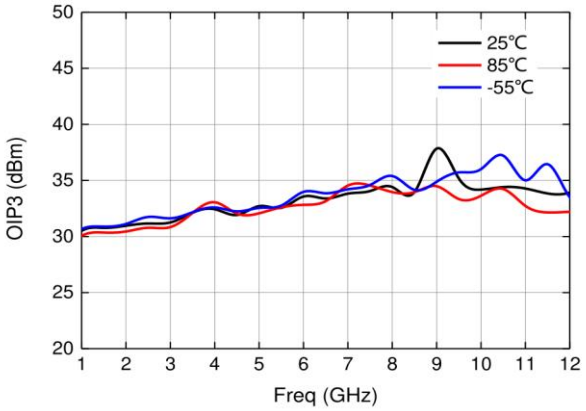


Output P-1dB vs. Frequency

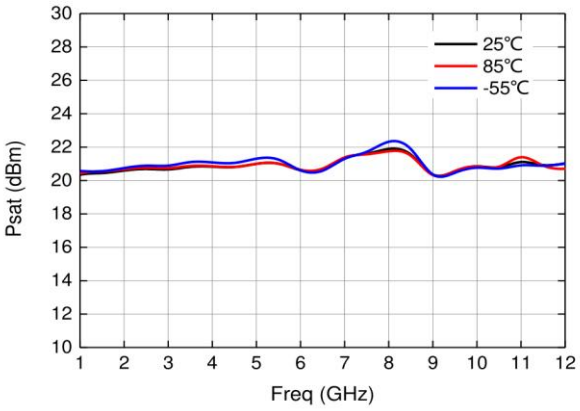


Email: ttf@ttfelectronic.com
Address: Building 16, Area C, Entrepreneurship and R&D Park, Xi'an High-tech Industrial Development Zone, China
Website:ttfelectronic.com

OIP3 vs. Frequency



Psat vs. Frequency



★5.Outline Dimensions



Notes:

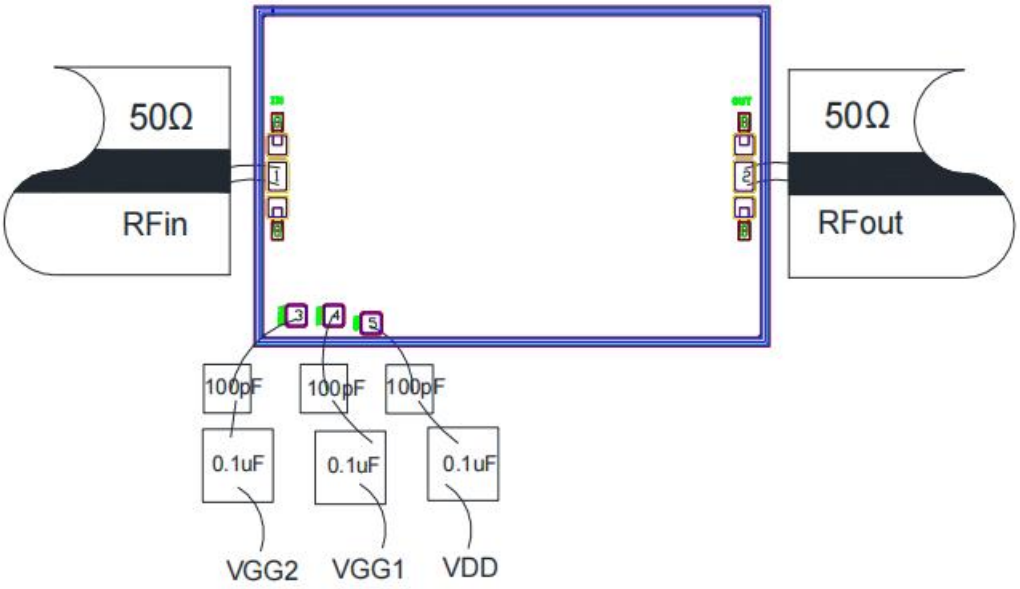
1. Unit: μm
2. Chip backside is gold-plated for grounding.
3. I/O pad size: 150 μm × 100 μm.
4. GND pad size: 100 μm × 100 μm.
5. Outline dimension tolerance: ±50 μm.

★6.Bonding Pressure Point Definition

Pressure Point Number	Function Definition	Function Description
1	RFin	RF signal input port, connected to an external 50Ω system. DC blocking is provided inside the chip.
2	RFout	RF signal output port, connected to an external 50Ω system. DC path to ground is provided inside the chip.
3	VGG2	Positive gate voltage supply port (+1.5 V).
4	VGG1	Negative gate voltage supply port (-0.47 V).
5	VDD	Drain voltage supply port (+5 V).
Other	GND	Ground bonding pad.

Email: ttf@ttfelectronic.com
Website:ttfelectronic.com
Address: Building 16, Area C, Entrepreneurship and R&D Park, Xi'an High-tech Industrial Development Zone, China

★7.Suggested Assembly Drawing



★8.Precautions

Parameter	Limit Value
Input Power (Pin, 50Ω)	+15 dBm
Drain Voltage	+7 V
Storage Temperature	-65℃~+150℃
Operating Temperature	-55℃~+125℃
Sintering Temperature (30s, N_2 Protection)	300℃
Exceeding any of the above conditions may cause permanent damage to the chip.	



This product is sensitive to static electricity.

Please take precautions against static electricity during use.

Email: ttf@ttfelectronic.com
Website:ttfelectronic.com
Address: Building 16, Area C, Entrepreneurship and R&D Park, Xi'an High-tech Industrial Development Zone, China