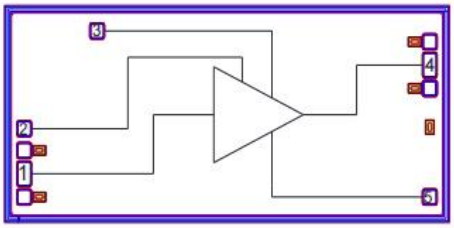
★1.Product Features

- Frequency range: 2 ~ 20 GHz
- Noise figure: 2.5 dB
- Gain: 15 dB
- Output P-1dB: 14 dBm
- Input return loss: -10 dB
- Output return loss: -10 dB
- Chip size: 3.1 mm × 1.35 mm × 0.1 mm
- Operating current: 60 mA

Functional Block Diagram



★2.Product Introduction

The TFLN1014-H is an ultra-wideband low noise amplifier chip operating in the 2~20 GHz frequency range with dual-supply operation. The typical gain is 15 dB, the noise figure is less than 2.5 dB, and the output power at 1 dB gain compression is greater than 14 dBm. It can be used in test instruments and radar T/R modules.

The chip backside is metallized and is suitable for eutectic bonding. The chip uses an on-chip metallized via process to ensure good grounding, requires no additional grounding measures, and is fabricated in a domestic GaAs process to meet localization requirements.

★3.Electrical Characteristics

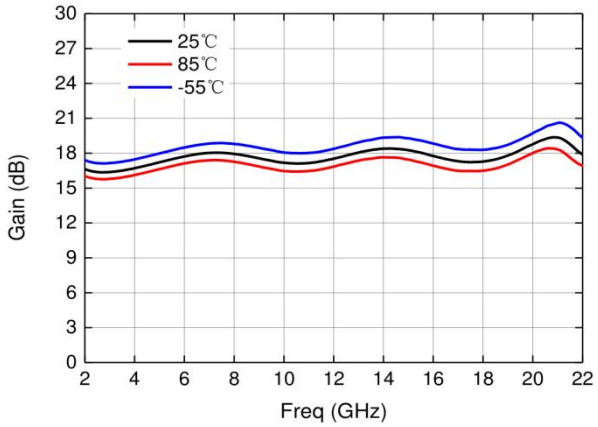
TA=+25℃, 50Ω System，VDD=+5V, VG1=-0.45V

Parameter	Symbol	Min	Typ	Max	Unit
Operating Frequency	Freq	2	—	20	GHz
Gain	Gain	—	15	—	dB
Gain Flatness	δGain	—	±1	—	dB
Noise Figure	NF	—	2.5	—	dB
Output P-1dB	OP1dB	—	14	—	dBm
Input Return Loss	RL_in	—	-10	—	dB
Output Return Loss	RL_out	—	-10	—	dB
Quiescent Current	IDQ*	—	60	—	mA
* Default VG1 = -0.45 V. In practice the VG voltage (-1.0 V ~ 0 V) shall be adjusted so that IDQ = 60 mA					

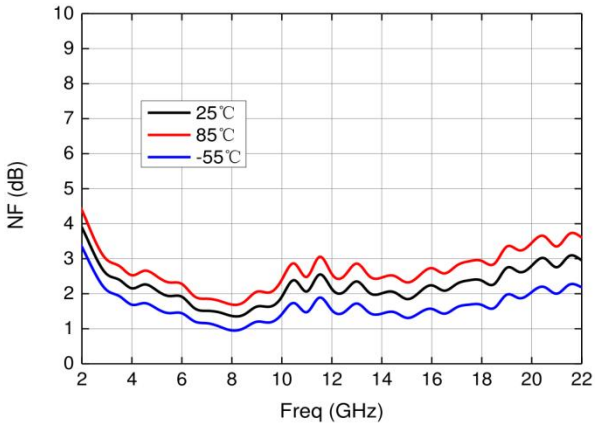
Email: ttf@ttfelectronic.com
Website:ttfelectronic.com
Address: Building 16, Area C, Entrepreneurship and R&D Park, Xi'an High-tech Industrial Development Zone, China

★4.Typical Test Curve

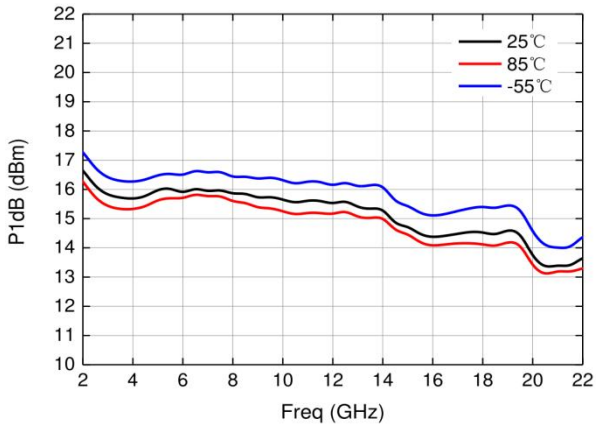
Gain vs. Frequency



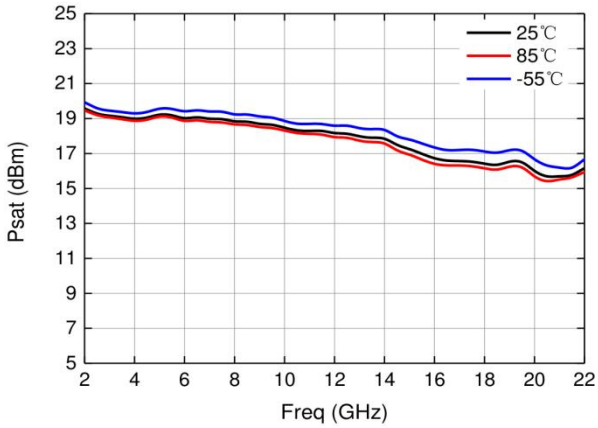
Noise Figure vs. Frequency



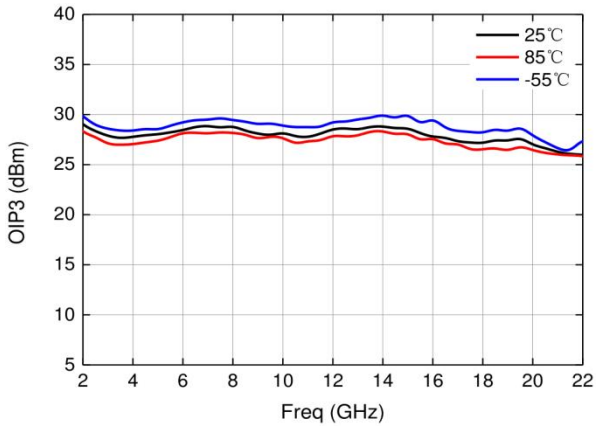
Output P-1dB vs. Frequency



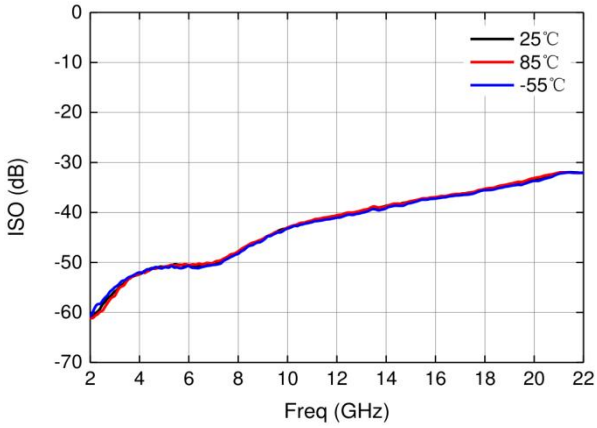
Saturated Output Power vs. Frequency



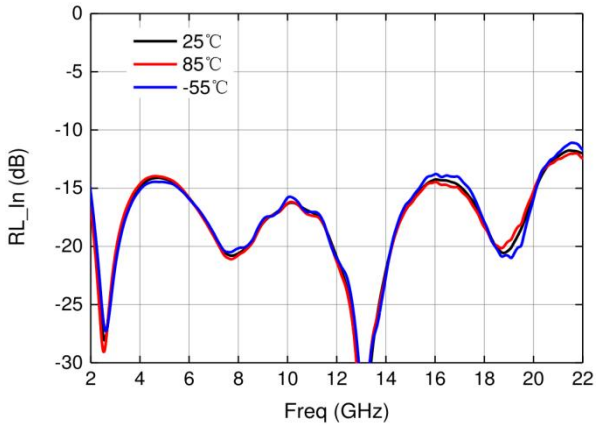
Output IP3 vs. Frequency



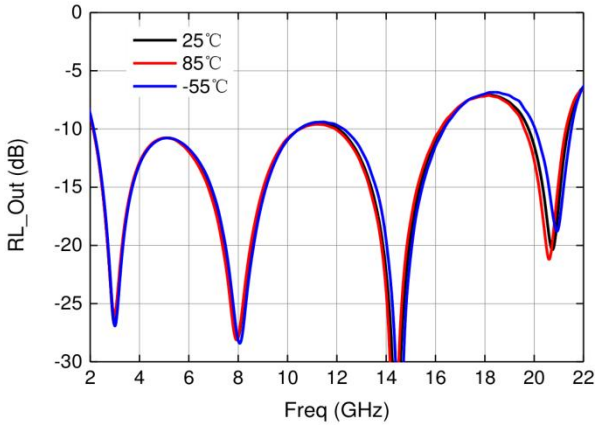
Reverse Isolation vs. Frequency



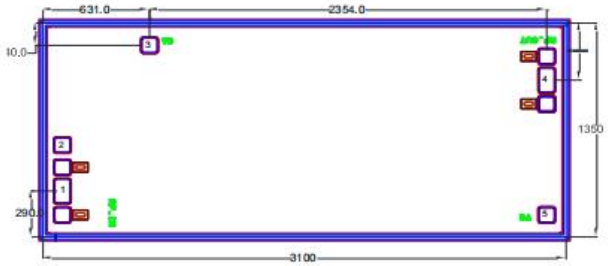
Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



★5.Outline Dimensions



Notes:
1. Unit: μm
2. Chip backside is gold-plated and grounded
3. RF pad size: 150 μm × 100 μm
4. DC pad size: 100 μm × 100 μm
5. Outline dimension tolerance: ±50 μm

★6.Bonding Pressure Point Definition

Pressure Point Number	Function Definition	Function Description
1	RFin	RF signal input port, connected to an external 50 Ω system, with internal DC_Block
2	VG2	Gain control port, voltage range: -1.2 V ~ 0 V
3	VD	Drain voltage supply port (+5 V)
4	RFout	RF signal output port, connected to an external 50 Ω system, with internal DC_Block
5	VG1	Gate negative voltage supply port

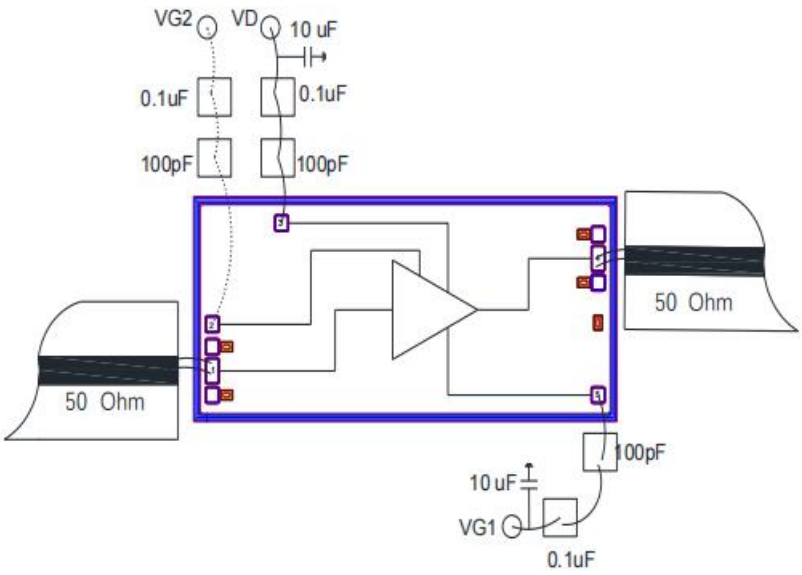
★7.Precautions

Parameter	Limit Value
Input Power (Pin, 50 Ω)	+15 dBm
Drain Voltage	+8 V
Storage Temperature	-65 ℃ ~ +150 ℃

Email: ttf@ttfelectronic.com
Address: Building 16, Area C, Entrepreneurship and R&D Park, Xi'an High-tech Industrial Development Zone, China
Website:ttfelectronic.com

Parameter	Limit Value
Operating Temperature	-55 ℃ ~ +85 ℃
Sintering Temperature (30 s, N_2 Protection)	300 ℃
Exceeding any of the above conditions may cause permanent damage to the chip	

★8.Suggested Assembly Drawing



Instructions for Use:

1. The RF ports are connected to 50 Ω microstrip lines with two 25 μm gold wires by wire bonding.
2. The filter capacitors are 100 pF chip capacitors, 0.1 μF ceramic capacitors and 10 μF tantalum capacitors by default. In practice the capacitance may be adjusted according to the supply noise.
3. Observe ESD precautions during chip assembly to avoid damage.
4. VG2 is the gain control port; if unused, a bypass capacitor shall be connected.



This product is sensitive to static electricity.
Please take precautions against static electricity during use.