★1.Product Features

- Utilizing GaAs technology, unlike silicon technology, no spurious signals
- Operating frequency range: DC ~ 8 GHz
- 0.5 dB LSB attenuation step, maximum attenuation 31.5 dB
- Insertion loss: 1.2 dB @ 800 MHz
- Input 1 dB compression point: +34 dBm @ 800 MHz
- Input third-order intermodulation point: +44.5dBm@800MHz
- +5V single-supply operation
- Package: QFN24 (plastic package)

Functional Block Diagram

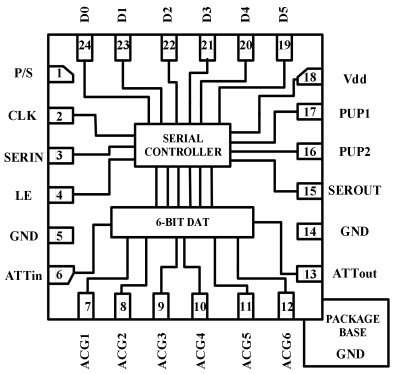


Figure 1 Functional block diagram (QFN24 package)

★2.Product Description

The TFDCA080TP is a wideband 6-bit serial/parallel digitally controlled attenuator chip designed using GaAs MMIC technology. This chip covers a frequency range of DC to 8 GHz and operates from a single +5V power supply. It achieves attenuation steps in 0.5 dB increments, with an attenuation range of 0.5 – 31.5 dB and a typical insertion loss of 1.2 dB. The six control pins represent attenuation increments of 0.5, 1, 2, 4, 8, and 16 dB, respectively. When all attenuation control bits are low, a full attenuation of 31.5 dB is achieved. The chip's dual-mode control interface is compatible with CMOS/TTL and supports three-wire serial input or 6-bit parallel words. The chip also provides selectable power-on states and a serial output port, allowing for cascading with other serial control components.

★3.Application

- Communication base stations
- Electronic countermeasures, remote sensing, and telemetry
- Shortwave and ultra-shortwave wireless communication equipment

Ordering Information

Table 1 Ordering information

Device Model	Packaging	Describe
TFDCA080TP	QFN24	DC~8GHz 6-bit serial-parallel digitally controlled attenuator

★4.Technical Specifications

Table 2 Electrical performance parameters

Parameters		Min	Typ	Max	Unit
Insertion loss Attenuation range	0.001GHz~3.0GHz	-0.8	- 1.2	- 1.9	dB
	3.0GHz~8.0GHz	- 1.5	-2.0	-2.8	
Input return loss	0.001GHz~8.0GHz	0.5	-	31.5	dB
Output return loss	0.001GHz~8.0GHz	-	- 15	-	dB
Insertion loss	0.001GHz~8.0GHz	-	- 15	-	dB
Attenuation accuracy: (Refer to insertion loss) All attenuation states	0.001GHz~1.0GHz 1.0GHz~4.0GHz 4.0GHz~6.0GHz 6.0GHz~8.0GHz	±0.6 ±0.3 ±0.4 ±0.3			dB
Input power 1 dB compression point	0.01 GHz~2.5 GHz	19. 1	34	34.9	dBm
Input power third-order intermodulation point	0.001GHz~4.2GHz	23. 1	44.5	48.5	dBm
Switching features Trise (50% CTL-90% RF) Tfall (50% CTL-10% RF)	200MHz 16 dB Attenuation Test	- -	71 78	- -	ns ns
Test conditions: Vdd=+5V, I=3mA, IIP3 spacing=1MHz, Pin=0dBm/tone, Temp=+25℃					

★5.Absolute Maximum Rating

- Maximum operating voltage (Vdd): +7V;
- Maximum RF input power: +27dBm (all attenuation states);
- Control voltage range: 0V~Vdd;

Note:

The absolute maximum rating indicates the limit that the device can withstand. Exceeding the absolute maximum rating may cause permanent damage to the device. Long-term operation under absolute maximum rating conditions will affect the reliability of the device.

★6.Recommended Operating Conditions

- Power Supply Voltage: +5V;
- Operating Current: 3mA;
- Control Voltage Threshold: 0~0.8V (Low Level); 2.7V~Vdd (High Level);
- PUP1/PUP2 Control Voltage Threshold: 0~0.8V (Low Level); Vdd-0.5~Vdd (High Level);
- Storage Temperature: -65℃~+150℃;
- Operating Temperature: -55℃~+125℃;

ESD Warning

This product is an electrostatic sensitive device. Appropriate ESD precautions should be taken to avoid performance degradation or loss of function.

★7.Typical Operating Characteristics

Table 3 Demo Board Test Results

Test Items	Typical value							Unit
Frequency	1	30	100	400	600	800	1000	MHz
Reference state insertion loss	-0.9	- 1. 1	- 1. 1	- 1.2	- 1.2	- 1.2	- 1.3	dB
Attenuation accuracy (0.5 dB)	0	0	0	0	0	-0. 1	0	dB
Attenuation accuracy (1 dB)	0	0	-0.1	0	0	-0. 1	0	dB
Attenuation accuracy (2 dB)	-0. 1	0	-0.1	-0.1	-0.1	-0. 1	-0. 1	dB
Attenuation accuracy (4 dB)	0	0	-0.1	-0.1	-0.1	-0. 1	-0. 1	dB
Attenuation accuracy (8 dB)	0.4	0.4	0.3	0. 1	0	0	0.1	dB
Attenuation accuracy (16 dB)	0.6	0.6	0.4	0. 1	0	-0. 1	-0. 1	dB
Attenuation accuracy (31.5 dB)	0.9	0.8	0.6	0. 1	-0.2	-0.6	-0.2	dB
Input Echo	- 19.0	-20.7	-20.7	- 19.7	- 19.0	- 18.5	- 18.5	dB
Output Echo	- 18.5	-20.5	-20.5	- 19.7	- 19.4	- 19. 1	- 19.2	dB
Input 1 dB Compression Point	-	20.9	23.5	33.4	33.5	34.0	34.3	dBm
Switch Time	80.6 ns Upward Switch				61.9 ns Downward switching			ns
Test conditions: Vdd=+5V, I=3mA, Temp=+25℃								

Test Items	Typical value							Unit
Frequency	1600	2000	2600	3000	3600	4000	4600	MHz
Reference state insertion loss	- 1.5	- 1.6	- 1.7	- 1.8	- 1.8	- 1.9	- 1.8	dB
Attenuation accuracy (0.5 dB)	0	0	0	0	0	0	-0. 1	dB
Attenuation accuracy (1 dB)	0	0	0	-0.1	0	0	-0.2	dB
Attenuation accuracy (2 dB)	-0. 1	0	-0.1	-0.1	-0.1	-0. 1	-0.2	dB
Attenuation accuracy (4 dB)	-0. 1	-0. 1	-0.1	-0.1	-0.1	-0. 1	-0.2	dB
Attenuation accuracy (8 dB)	0.1	0. 1	0. 1	0. 1	0. 1	0. 1	-0. 1	dB
Attenuation accuracy (16 dB)	0	-0. 1	-0.1	-0.1	0	-0. 1	-0.3	dB
Attenuation accuracy (31.5 dB)	-0.2	-0. 1	-0.2	-0.3	-0.5	-0.7	-0.4	dB
Input Echo	- 19. 1	-20.5	-20.0	- 18.3	- 19.3	-22.4	-31.4	dB

Output Echo	-20.5	-21.5	- 19.0	- 17.2	- 16.7	- 19.0	-30.6	dB
Input 1 dB Compression Point	34.6	34.9	-	-	-	-	-	dBm
Switch Time	80.6 ns Upward Switch				61.9 ns Downward switching			ns
Test conditions: Vdd=+5V, I=3mA, Temp=+25℃								

Test items	**Typical value**							**Unit**
Frequency	5000	5600	6000	6600	7000	7600	8000	MHz
Reference state insertion loss	-2.1	-2.3	-2.8	-2.7	-2.2	-2.6	-2.3	dB
Attenuation accuracy (0.5 dB)	0	0	0	0. 1	0. 1	0	0	dB
Attenuation accuracy (1 dB)	-0. 1	-0. 1	0	0. 1	0	-0. 1	-0. 1	dB
Attenuation accuracy (2 dB)	-0.2	-0. 1	0	0. 1	0	-0. 1	-0. 1	dB
Attenuation accuracy (4 dB)	-0.2	-0. 1	0	0. 1	0	0	0	dB
Attenuation accuracy (8 dB)	-0.2	-0. 1	0.2	0.3	0.2	0.2	0.3	dB
Attenuation accuracy (16 dB)	-0.3	-0. 1	0. 1	0.3	0.3	0.3	0.5	dB
Attenuation accuracy (31.5 dB)	-0.7	-0.2	-0.2	0.3	0	0.3	0.6	dB
Input Echo	-20.7	- 13.4	- 11.4	- 11.1	- 12.6	- 19.7	-25.2	dB
Output Echo	-22.7	- 14.5	- 11.8	- 11.1	- 12.6	- 18.4	-21.3	dB
Input 1 dB Compression Point	-	-	-	-	-	-	-	dBm
Switch Time	80.6 ns Upward Switch				61.9 ns Downward switching			ns
Test conditions: Vdd=+5V, I=3mA, Temp=+25℃								

★8.Test Curve

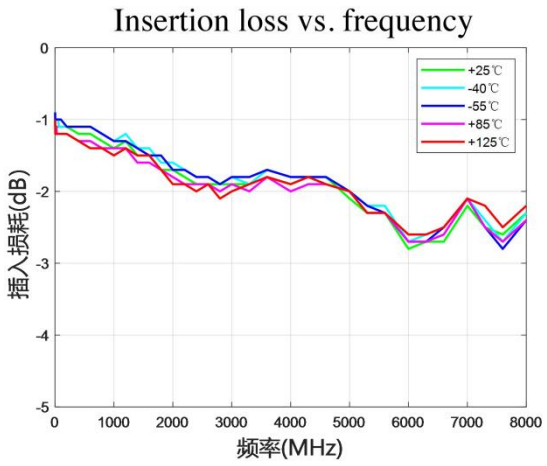


Figure 2 Insertion loss

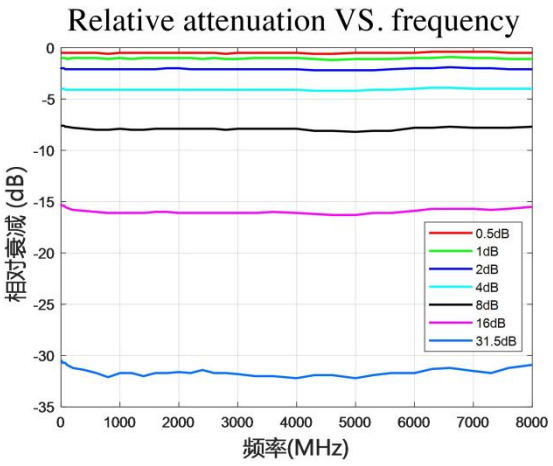


Figure 3 Relative attenuation

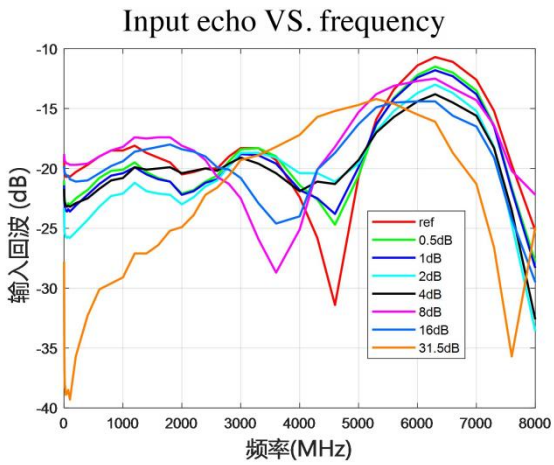


Figure 4 Input echo

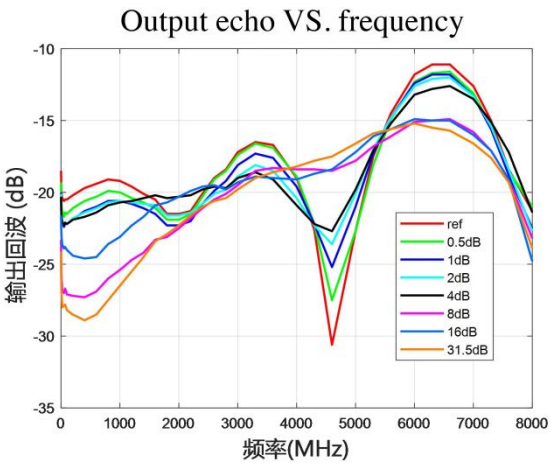


Figure 5 Output echo

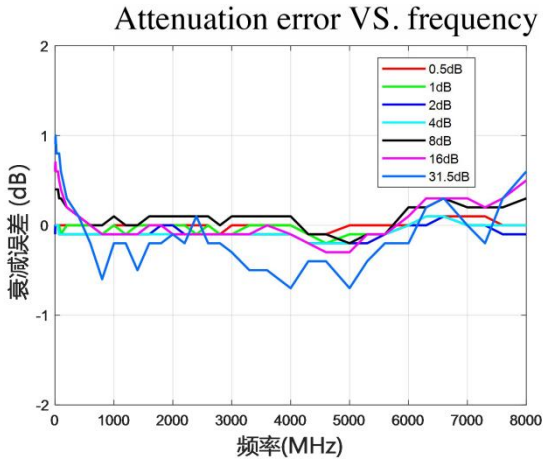


Figure 6 Attenuation error

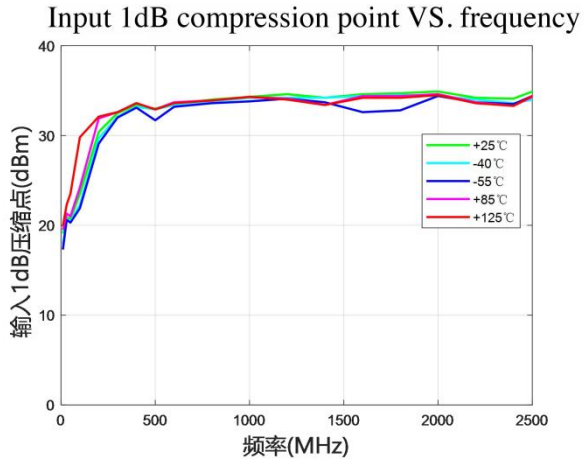


Figure 7 Input 1 dB compression point

★9.Typical Application Circuits

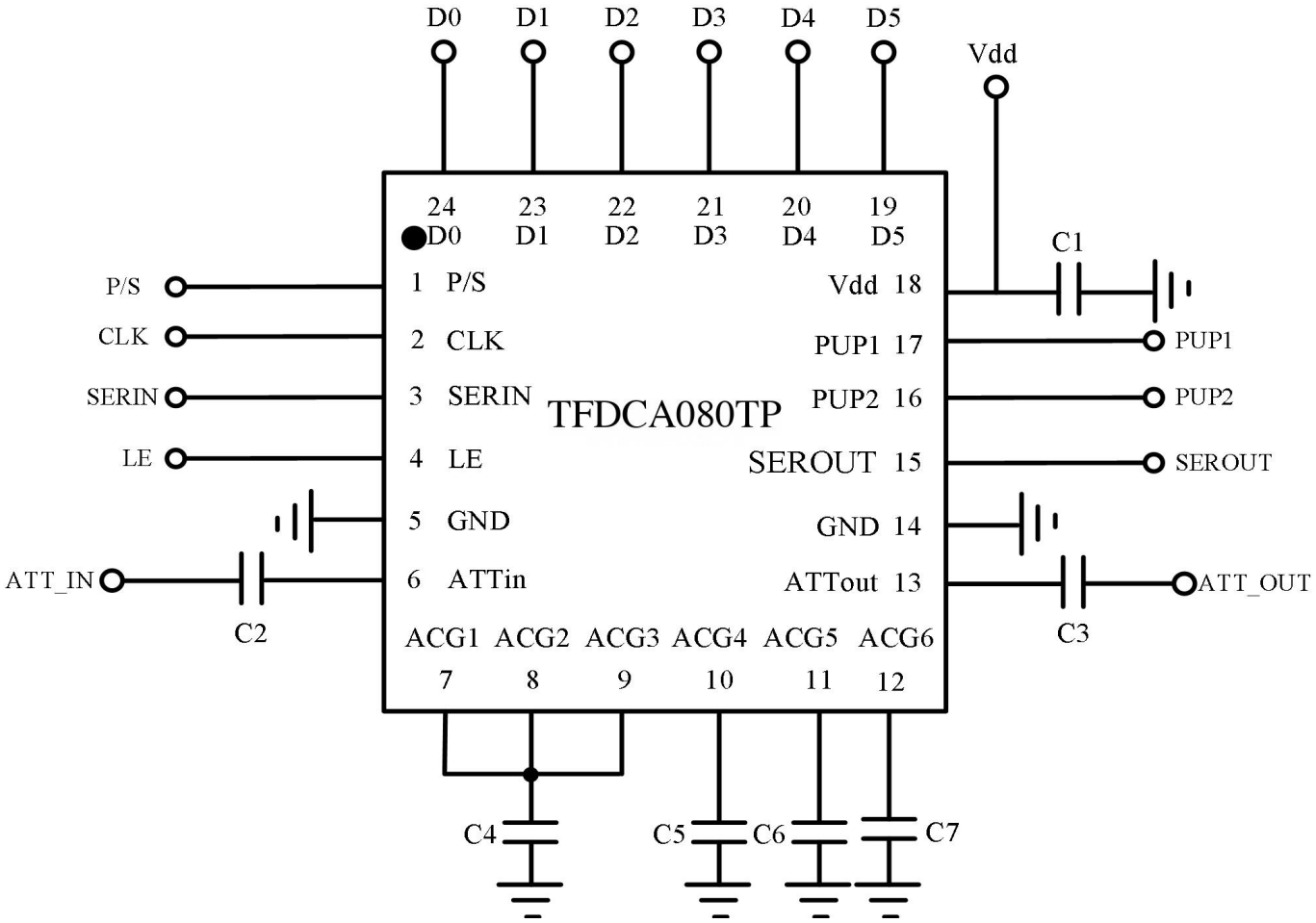
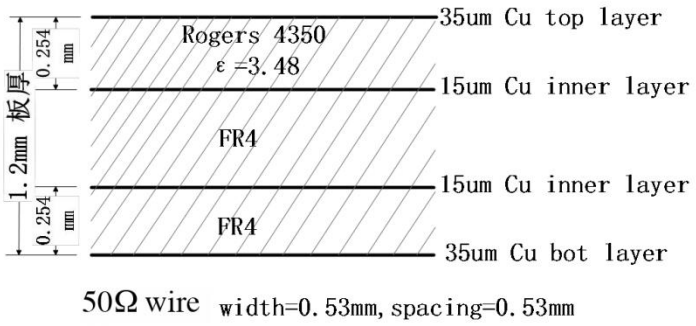


Figure 8: Typical application circuit diagram

★10.Evaluation Board Information

PCB Parameter Information



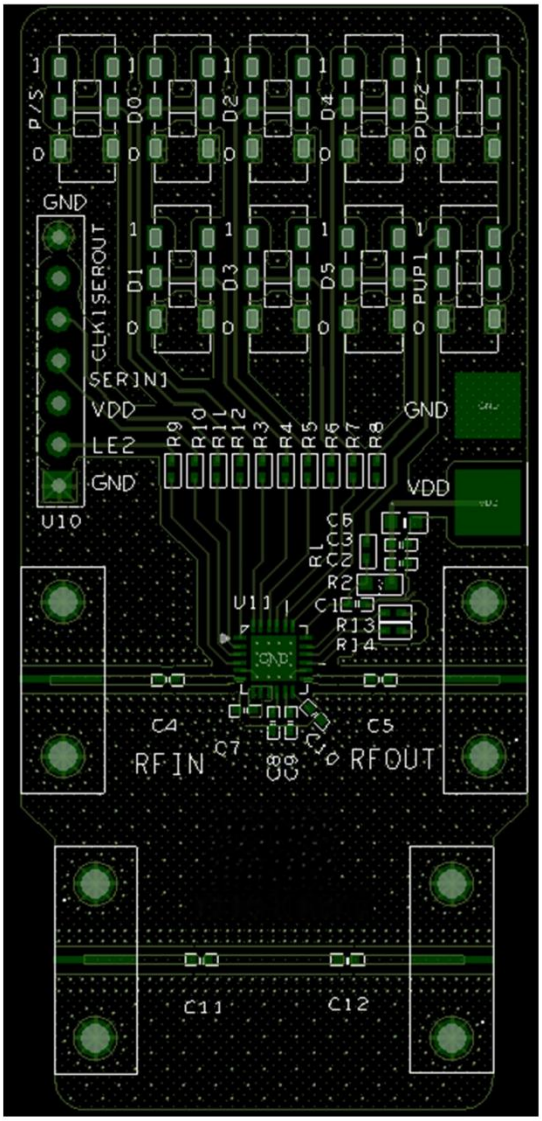


Figure 9 Evaluation Board Information

★11.Pin Function Description

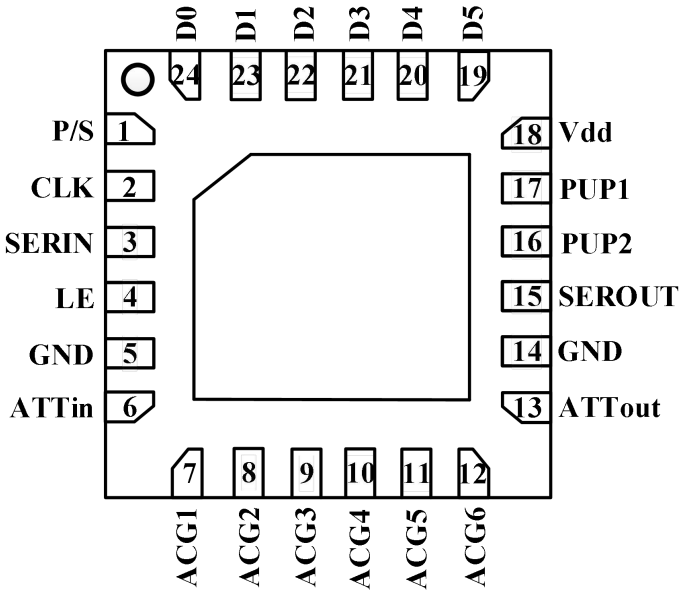


Figure 10 Pin Arrangement

Table 4 Pin Description

Pin number	Pin name	Describe
1	P/S	Serial/parallel control pin. P/S=0 indicates parallel operation, and P/S=1 indicates serial operation.
5, 14	GND	Ground pin; this pin and the package substrate must be connected to RF/DC ground.
7 ~ 12	ACG1~ACG6	The capacitor is grounded at the pin, and its capacitance value is determined by the lowest operating frequency. The capacitor should be placed as close to the pin as possible.
6, 13	ATTin ATTout	This pin is DC coupled and matched to 50 ohms, requiring an external DC blocking capacitor. The capacitance value is determined by the minimum operating frequency.
15	SEROUT	The serial input data is output from this pin after a lag of 6 clock cycles.
19 ~ 24	D5~D0	Parallel control is described in the control truth table. When parallel control pins are not suitable, the parallel port needs to be pulled up or down.
2	CLK	Serial control clock pin.
3	SERIN	Serial input data pin.
4	LE	Serial enable pin.
16, 17	PUP2, PUP1	Power-on status control pin.
18	Vdd	Power supply voltage pin.
-	EP	Grounding.

★12. Chip Status Selection

The TFDCA080TP employs three control methods: power-on control, serial control, and parallel control. The control pins and truth tables for these three states are shown in Table 5.

Table 5 Truth Table for Chip State Selection Control

LE	P/S	Chip Status
0	X	Power-On Control
1	0	Parallel Control
1	1	Serial Control

(1) Power-On State

If the LE pin is set low upon power-on, the output logic state depends on the levels of PUP1 and PUP2, as shown in Table 6 of the PUP truth table.

Table 6: PUP Truth Table

LE	PUP1	PUP2	Relative attenuation setting
0	0	0	-31.5dB
0	1	0	-24dB
0	0	1	- 16 dB
0	1	1	Insertion loss
1	X	X	Serial/Parallel Control

(2) Serial control

The TFDCA080TP is controlled by a 3-wire SPI (SERIN, CLK, LE) digitally compatible interface. SPI operation is active when P/S = 1; during normal operation, P/S is high. The 6-bit serial data is first loaded into the MSB; the rising edge triggers CLK and LE to be cleared and switched; the 6-bit serial data is sequentially sent to the register and output to the attenuator. Simultaneously, CLK is masked to prevent changes in the output state; except for power-on PUP1 and PUP2 control, the output remains unchanged when LE = 0 for all other operations.

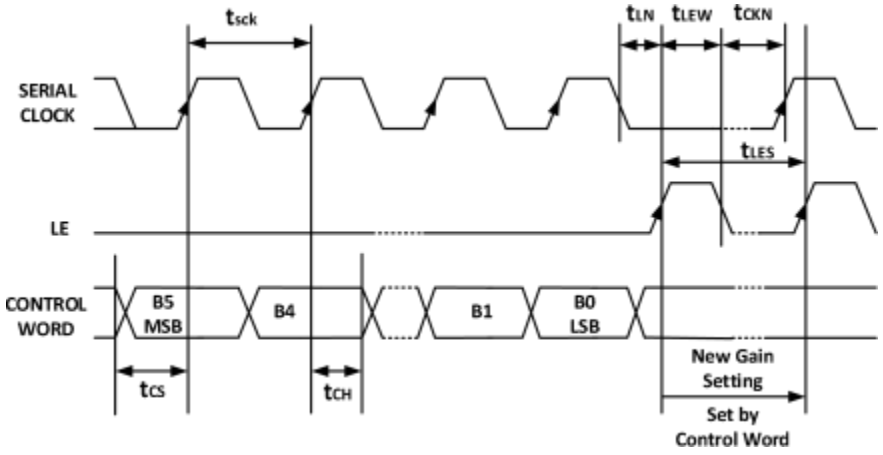


Figure 11 Serial control logic diagram

Table 7 Timing Characteristics

Serial Number	Parameter	Typical value
1	Minimum clock period (tSCK)	100ns
2	Control signal setup time (tCS)	20ns
3	Control signal hold time (tCH)	20ns
4	LE signal setup time (tLN)	10ns
5	Minimum LE pulse duration (tLEW)	10ns
6	Minimum LE pulse interval (tLES)	630ns
7	Serial clock hold time (tCKN) starting from LE	10ns

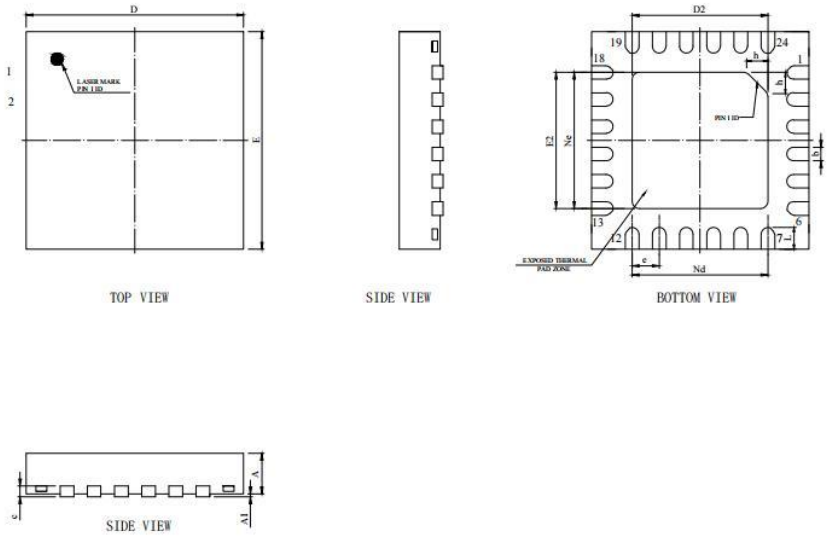
(3) Parallel control

When using parallel control, LE = 1, P/S = 0, and the control truth table is as follows:

Table 8 Truth Table of Parallel Control Voltage

Control voltage input						Decay state RF1/RF2
D5 16dB	D4 8dB	D3 4dB	D2 2dB	D1 1dB	D0 0.5dB	
1	1	1	1	1	1	Reference state insertion loss
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB
Note: Any combination of the above attenuation states can provide an attenuation amount approximately equal to the sum of the attenuations of the selected bits.						

★13.Package Information (Unit: mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.80	0.85
A1	0.01	0.02	0.05
b	0.20	0.25	0.30
c		0.270REF	
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
L	0.35	0.40	0.45
h	0.35	0.40	0.45

Figure 12 Packaging Information Diagram